

**Project Name :VEXSN81**  
**Platform : SKL\_H+N17E**

PAGE	TITLE	PAGE	TITLE
01	INDEX	41	+1.2VS/+2.5VS
02	System Block Diagram	42	VCCGT / VCORE
03	Power Block Diagram	43	VCCSA
04	GPIO Table & SMBUS Block	44	TP/LED/WEBCAM/USB
05	CPU SKL-H : DDR4 CH-A	45	PCIE to USB3.1(ASM1142)
06	CPU SKL-H : DDR4 CH-B	46	GFX-PCIE
07	CPU SKL-H : PEG/DMI	47	FrameBuffer AB
08	CPU SKL-H : DDI/EDP	48	FrameBuffer A_VRAM
09	CPU SKL-H : MISC/CLK/JTAG/CF	49	FrameBuffer B_VRAM
10	CPU SKL-H : GND	50	Frame Buffer CD
11	CPU SKL-H : VCC	51	Frame Buffer C_VRAM
12	CPU SKL-H : VCCGT	52	Frame Buffer D_VRAM
13	CPU SKL-H : VCCSA/VCCIO/VDDQ	53	PEX_VDD/3V3_ON/1.8V
14	CPU SKL-H : VCCOPC/RSVD	54	GFX_NVVDD_CONTROLLER
15	CPU SKL-H : RSVD	55	GFX_NVVDD_PHASE1_4
16	PCH SKL-H : SPI	56	GFX POWER
17	PCH SKL-H : DMI/PCIE/USB	57	GFX NVVDD /PWR MEAS
18	PCH SKL-H : SATA/PCIE	58	Decoupling capacitor /FBVDDQ
19	PCH SKL-H : AUDIO/SMBUS/JTAG	59	Unused IPFA_B_C_D_E_F
20	PCH SKL-H : DDI CONTROL	60	BIOS,XTAL ,External SS ,M
21	PCH SKL-H : USB3/LPC	61	GPIO, Thermal Sensor, I2C
22	PCH SKL-H : CLK	62	STRAP
23	PCH SKL-H : POWER	63	Thermal IC/RGB
24	PCH SKL-H : GSPI/UART/I2C	64	Change list
25	PCH SKL-H : GND/RSVD	65	History
26	DDR4 SODIMM-A	66	
27	DDR4 SODIMM-B	67	
28	eDP panel	68	
29	HDMI/DisplayPort	69	
30	EC(IT8528E)/BIOS/KB_CONN	70	
31	PSW/Q Key		
32	HDD/ODD/MINI_CARD		
33	LAN_PHY(RTL8118AG)		
34	CODEC(ALC269Q)/INT_MIC/SPKR		
35	EXT_MIC/USB/FAN/G-sen		
36	BATT_IN/CHARGER(OZ8686)		
37	DC_IN/D-Resis/HOLE/Debug		
38	+5VA/+3.3VAL		
39	+1.0VA_PCH/VCCIO		
40	VCC_SW		

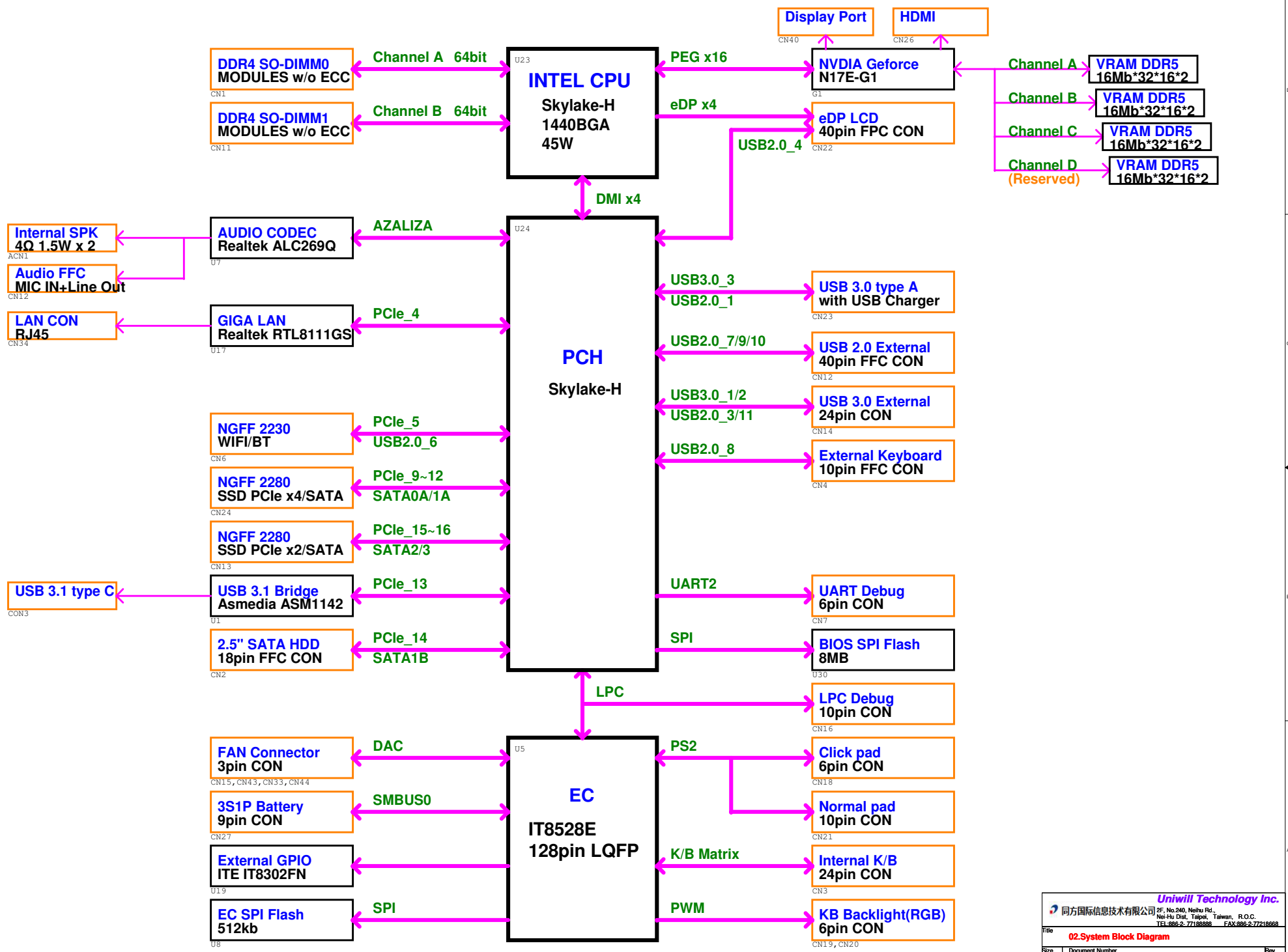
## M/B Schematic Version Change List

[illegible]

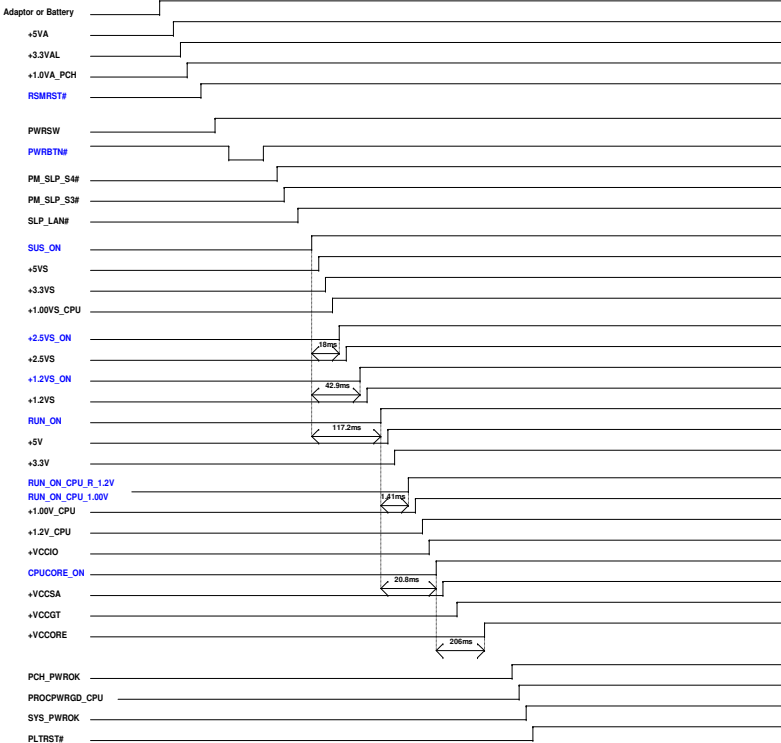
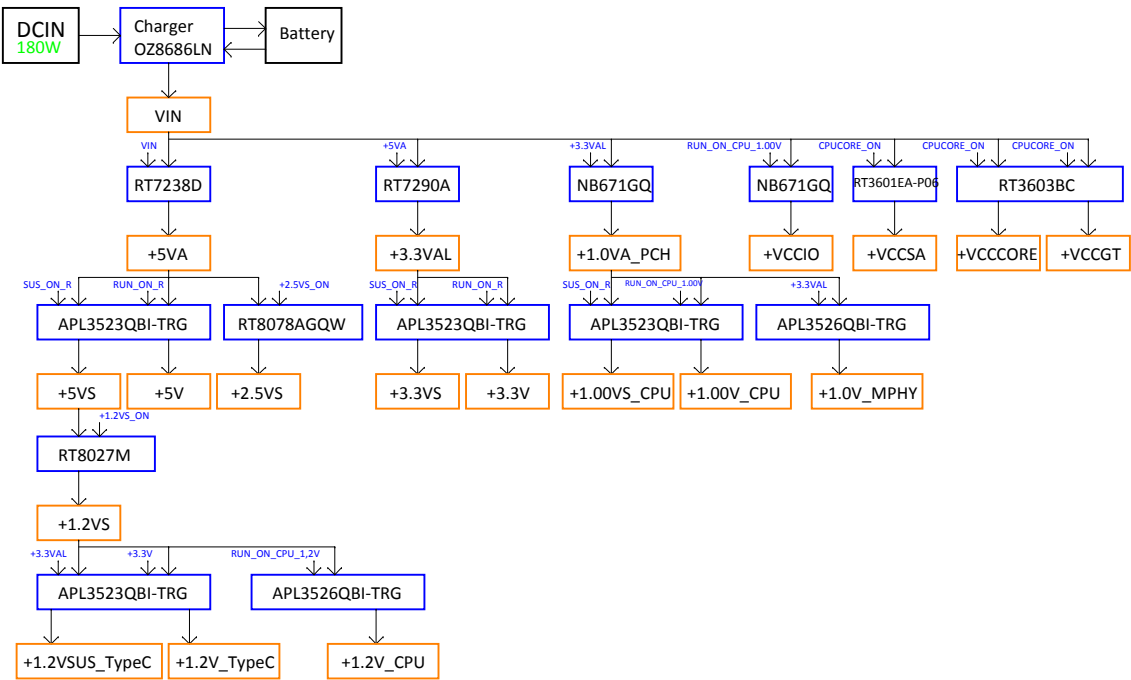
## Daughter Board Schematic Version Change List

[illegible]

SYSTEM BLOCK DIAGRAM



POWER BLOCK DIAGRAM



Pin#	Function2	Function3	GPIO	Pin	Function	Net Name	Internal PUPD	External PUPD	Active
PWM0	WU43		GP0	24	PWM	PWM_KB_LED_G			
PWM1	WU44		GP1	25	PWM	PWM_KB_LED_G			
PWM2	WU45		GP2	28	PWM	PWM_KB_LED_B			
PWM3	WU32		GP3	29	PWM	PWM_KB_LED_R			
PWM4	WU33		GP4	30	PWM	PID_1_CHD_R_LED			
PWM5	WU34		GP5	31	PWM	PID_2_PWR_LED			
PWM6	WU35		GP6	32	PWM	ME_KB_LED			
PWM7	WU52	SSCK	GP7	34	x				
		RXT1#	GP8						
			GP9						
			GP10						
			GP11						
			GP12						
			GP13						
			GP14						
			GP15						
			GP16						
			GP17						
			GP18						
			GP19						
			GP20						
			GP21						
			GP22						
			GP23						
			GP24						
			GP25						
			GP26						
			GP27						
			GP28						
			GP29						
			GP30						
			GP31						
			GP32						
			GP33						
			GP34						
			GP35						
			GP36						
			GP37						
			GP38						
			GP39						
			GP40						
			GP41						
			GP42						
			GP43						
			GP44						
			GP45						
			GP46						
			GP47						
			GP48						
			GP49						
			GP50						
			GP51						
			GP52						
			GP53						
			GP54						
			GP55						
			GP56						
			GP57						
			GP58						
			GP59						
			GP60						
			GP61						
			GP62						
			GP63						
			GP64						
			GP65						
			GP66						
			GP67						
			GP68						
			GP69						
			GP70						
			GP71						
			GP72						
			GP73						
			GP74						
			GP75						
			GP76						

[26] M\_A DQ0  
[26] M\_A DQ1  
[26] M\_A DQ2  
[26] M\_A DQ3  
[26] M\_A DQ4  
[26] M\_A DQ5  
[26] M\_A DQ6  
[26] M\_A DQ7  
[26] M\_A DQ8  
[26] M\_A DQ9  
[26] M\_A DQ10  
[26] M\_A DQ11  
[26] M\_A DQ12  
[26] M\_A DQ13  
[26] M\_A DQ14  
[26] M\_A DQ15  
[26] M\_A DQ16  
[26] M\_A DQ17  
[26] M\_A DQ18  
[26] M\_A DQ19  
[26] M\_A DQ20  
[26] M\_A DQ21  
[26] M\_A DQ22  
[26] M\_A DQ23  
[26] M\_A DQ24  
[26] M\_A DQ25  
[26] M\_A DQ26  
[26] M\_A DQ27  
[26] M\_A DQ28  
[26] M\_A DQ29  
[26] M\_A DQ30  
[26] M\_A DQ31  
[26] M\_A DQ32  
[26] M\_A DQ33  
[26] M\_A DQ34  
[26] M\_A DQ35  
[26] M\_A DQ36  
[26] M\_A DQ37  
[26] M\_A DQ38  
[26] M\_A DQ39  
[26] M\_A DQ40  
[26] M\_A DQ41  
[26] M\_A DQ42  
[26] M\_A DQ43  
[26] M\_A DQ44  
[26] M\_A DQ45  
[26] M\_A DQ46  
[26] M\_A DQ47  
[26] M\_A DQ48  
[26] M\_A DQ49  
[26] M\_A DQ50  
[26] M\_A DQ51  
[26] M\_A DQ52  
[26] M\_A DQ53  
[26] M\_A DQ54  
[26] M\_A DQ55  
[26] M\_A DQ56  
[26] M\_A DQ57  
[26] M\_A DQ58  
[26] M\_A DQ59  
[26] M\_A DQ60  
[26] M\_A DQ61  
[26] M\_A DQ62  
[26] M\_A DQ63

BR6 DDR0\_DQ[0]  
BT6 DDR0\_DQ[1]  
BP3 DDR0\_DQ[2]  
BR3 DDR0\_DQ[3]  
BN5 DDR0\_DQ[4]  
BP6 DDR0\_DQ[5]  
BP2 DDR0\_DQ[6]  
BN3 DDR0\_DQ[7]  
BL4 DDR0\_DQ[8]  
BL5 DDR0\_DQ[9]  
BL2 DDR0\_DQ[10]  
BM1 DDR0\_DQ[11]  
BK4 DDR0\_DQ[12]  
BK5 DDR0\_DQ[13]  
BK1 DDR0\_DQ[14]  
BK2 DDR0\_DQ[15]  
BG4 DDR0\_DQ[16]/DDR0\_DQ[32]  
BF4 DDR0\_DQ[17]/DDR0\_DQ[33]  
BF5 DDR0\_DQ[18]/DDR0\_DQ[34]  
BG2 DDR0\_DQ[19]/DDR0\_DQ[35]  
BG1 DDR0\_DQ[20]/DDR0\_DQ[36]  
BF1 DDR0\_DQ[21]/DDR0\_DQ[37]  
BF2 DDR0\_DQ[22]/DDR0\_DQ[38]  
BD2 DDR0\_DQ[23]/DDR0\_DQ[39]  
BD1 DDR0\_DQ[24]/DDR0\_DQ[40]  
BC4 DDR0\_DQ[25]/DDR0\_DQ[41]  
BC5 DDR0\_DQ[26]/DDR0\_DQ[42]  
BD5 DDR0\_DQ[27]/DDR0\_DQ[43]  
BD4 DDR0\_DQ[28]/DDR0\_DQ[44]  
BC1 DDR0\_DQ[29]/DDR0\_DQ[45]  
BC2 DDR0\_DQ[30]/DDR0\_DQ[46]  
BD1 DDR0\_DQ[31]/DDR0\_DQ[47]  
AB1 DDR0\_DQ[32]/DDR1\_DQ[0]  
AB2 DDR0\_DQ[33]/DDR1\_DQ[1]  
AA4 DDR0\_DQ[34]/DDR1\_DQ[2]  
AA5 DDR0\_DQ[35]/DDR1\_DQ[3]  
AB5 DDR0\_DQ[36]/DDR1\_DQ[4]  
AB4 DDR0\_DQ[37]/DDR1\_DQ[5]  
AA2 DDR0\_DQ[38]/DDR1\_DQ[6]  
AA1 DDR0\_DQ[39]/DDR1\_DQ[7]  
V5 DDR0\_DQ[40]/DDR1\_DQ[8]  
V2 DDR0\_DQ[41]/DDR1\_DQ[9]  
U1 DDR0\_DQ[42]/DDR1\_DQ[10]  
U2 DDR0\_DQ[43]/DDR1\_DQ[11]  
V1 DDR0\_DQ[44]/DDR1\_DQ[12]  
V4 DDR0\_DQ[45]/DDR1\_DQ[13]  
U5 DDR0\_DQ[46]/DDR1\_DQ[14]  
U4 DDR0\_DQ[47]/DDR1\_DQ[15]  
R2 DDR0\_DQ[48]/DDR1\_DQ[32]  
P5 DDR0\_DQ[49]/DDR1\_DQ[33]  
R4 DDR0\_DQ[50]/DDR1\_DQ[34]  
P4 DDR0\_DQ[51]/DDR1\_DQ[35]  
R5 DDR0\_DQ[52]/DDR1\_DQ[36]  
P2 DDR0\_DQ[53]/DDR1\_DQ[37]  
R1 DDR0\_DQ[54]/DDR1\_DQ[38]  
M4 DDR0\_DQ[55]/DDR1\_DQ[39]  
M1 DDR0\_DQ[56]/DDR1\_DQ[40]  
L4 DDR0\_DQ[57]/DDR1\_DQ[41]  
L2 DDR0\_DQ[58]/DDR1\_DQ[42]  
M5 DDR0\_DQ[59]/DDR1\_DQ[43]  
M2 DDR0\_DQ[60]/DDR1\_DQ[44]  
L5 DDR0\_DQ[61]/DDR1\_DQ[45]  
L1 DDR0\_DQ[62]/DDR1\_DQ[46]  
L1 DDR0\_DQ[63]/DDR1\_DQ[47]  
BA2 DDR0\_ECC[0]  
BA1 DDR0\_ECC[1]  
AY4 DDR0\_ECC[2]  
AY5 DDR0\_ECC[3]  
BA5 DDR0\_ECC[4]  
BA4 DDR0\_ECC[5]  
AY1 DDR0\_ECC[6]  
AY2 DDR0\_ECC[7]

DDR CHANNEL A

SKL\_H\_BGA\_BGA  
REV = 1

SKYLAKE\_HA20  
BGA1440

DDR0\_CKP[0]  
DDR0\_CKN[0]  
DDR0\_CKN[1]  
DDR0\_CKP[1]  
DDR0\_CLKP[2]  
DDR0\_CLKN[2]  
DDR0\_CLKP[3]  
DDR0\_CLKN[3]  
DDR0\_CKE[0]  
DDR0\_CKE[1]  
DDR0\_CKE[2]  
DDR0\_CKE[3]  
DDR0\_CS#0  
DDR0\_CS#1  
DDR0\_CS#2  
DDR0\_CS#3  
DDR0\_ODT[0]  
DDR0\_ODT[1]  
DDR0\_ODT[2]  
DDR0\_ODT[3]  
DDR0\_BA[0]/DDR0\_CAB[4]/DDR0\_BA[0]  
DDR0\_BA[1]/DDR0\_CAB[6]/DDR0\_BA[1]  
DDR0\_BA[2]/DDR0\_CAA[5]/DDR0\_BG[0]  
DDR0\_RAS#/DDR0\_CAB[3]/DDR0\_MA[16]  
DDR0\_WE#/DDR0\_CAB[2]/DDR0\_MA[14]  
DDR0\_CAS#/DDR0\_CAB[1]/DDR0\_MA[15]  
DDR0\_MA[0]/DDR0\_CAB[9]/DDR0\_MA[0]  
DDR0\_MA[1]/DDR0\_CAB[8]/DDR0\_MA[1]  
DDR0\_MA[2]/DDR0\_CAB[5]/DDR0\_MA[2]  
DDR0\_MA[3]  
DDR0\_MA[4]  
DDR0\_MA[5]/DDR0\_CAA[0]/DDR0\_MA[5]  
DDR0\_MA[6]/DDR0\_CAA[2]/DDR0\_MA[6]  
DDR0\_MA[7]/DDR0\_CAA[4]/DDR0\_MA[7]  
DDR0\_MA[8]/DDR0\_CAA[3]/DDR0\_MA[8]  
DDR0\_MA[9]/DDR0\_CAA[1]/DDR0\_MA[9]  
DDR0\_MA[10]/DDR0\_CAB[7]/DDR0\_MA[10]  
DDR0\_MA[11]/DDR0\_CAA[7]/DDR0\_MA[11]  
DDR0\_MA[12]/DDR0\_CAA[6]/DDR0\_MA[12]  
DDR0\_MA[13]/DDR0\_CAB[0]/DDR0\_MA[13]  
DDR0\_MA[14]/DDR0\_CAA[9]/DDR0\_BG[1]  
DDR0\_MA[15]/DDR0\_CAA[8]/DDR0\_ACT#  
DDR0\_PAR  
DDR0\_ALERT#  
DDR0\_DQSN[0]  
DDR0\_DQSN[1]  
DDR0\_DQSN[2]/DDR0\_DQSN[4]  
DDR0\_DQSN[3]/DDR0\_DQSN[5]  
DDR0\_DQSP[4]/DDR1\_DQSP[0]  
DDR0\_DQSP[5]/DDR1\_DQSP[1]  
DDR0\_DQSP[6]/DDR1\_DQSP[4]  
DDR0\_DQSP[7]/DDR1\_DQSP[5]  
DDR0\_DQSP[0]  
DDR0\_DQSP[1]  
DDR0\_DQSP[2]/DDR0\_DQSP[4]  
DDR0\_DQSP[3]/DDR0\_DQSP[5]  
DDR0\_DQSN[4]/DDR1\_DQSN[0]  
DDR0\_DQSN[5]/DDR1\_DQSN[1]  
DDR0\_DQSN[6]/DDR1\_DQSN[3]  
DDR0\_DQSN[7]/DDR1\_DQSN[5]  
DDR0\_DQSP[8]  
DDR0\_DQSN[8]

AG1  
AG2  
AK1  
AK2  
AL3  
AK3  
AL2  
AL1  
AT1  
AT2  
AT3  
AT5  
AD5  
AE2  
AD2  
AE5  
AD3  
AE4  
AE1  
AD4  
AH5  
AH1  
AU1  
AH4  
AG4  
AD1  
AH3  
AP4  
AN4  
AP5  
AP2  
AP1  
AP3  
AN1  
AN3  
AT4  
AH2  
AN2  
AU4  
AE3  
AU2  
AU3  
AG3  
AU5  
BR5  
BL3  
BG3  
BD3  
AB3  
V3  
R3  
M3  
BP5  
BK3  
BF3  
BC3  
AA3  
U3  
P3  
L3  
AY3  
BA3

Correct CLK1 P/N  
Sun 12/9

MA\_CLK0 [26]  
MA\_CLK#0 [26]  
MA\_CLK#1 [26]  
MA\_CLK1 [26]

change DDR0\_CKP/N (2,3) to (1,0)

MA\_CKE0 [26]  
MA\_CKE1 [26]

change DDR0\_CKE (2,3) to (1,0)

MA\_CS#0 [26]  
MA\_CS#1 [26]

change DDR0\_CS# (2,3) to (1,0)

MA\_ODT0 [26]  
MA\_ODT1 [26]

change DDR0\_ODT (2,3) to (1,0)

NPI modify---Leon 11/27

M\_A BA0 [26]  
M\_A BA1 [26]  
M\_A BG0 [26]

M\_A A16\_MA\_RAS# [26]  
M\_A A14\_MA\_WE# [26]  
M\_A A15\_MA\_CAS# [26]

M\_A A0 [26]  
M\_A A1 [26]  
M\_A A2 [26]  
M\_A A3 [26]  
M\_A A4 [26]  
M\_A A5 [26]  
M\_A A6 [26]  
M\_A A7 [26]  
M\_A A8 [26]  
M\_A A9 [26]

M\_A A10\_AP [26]  
M\_A A11 [26]  
M\_A A12 [26]  
M\_A A13 [26]  
M\_A BG1 [26]  
M\_A\_ACT\_N [26]

DDR0\_A\_PARITY [26]  
DDR0\_A\_ALERT\_N [26]

M\_A DQS#0 [26]  
M\_A DQS#1 [26]  
M\_A DQS#2 [26]  
M\_A DQS#3 [26]  
M\_A DQS4 [26]  
M\_A DQS5 [26]  
M\_A DQS6 [26]  
M\_A DQS7 [26]

M\_A DQSO [26]  
M\_A DQS1 [26]  
M\_A DQS2 [26]  
M\_A DQS3 [26]  
M\_A DQS#4 [26]  
M\_A DQS#5 [26]  
M\_A DQS#6 [26]  
M\_A DQS#7 [26]

Uniwill Technology Inc.

同方国际信息技术有限公司

2F, No.240, Neihu Rd.,  
Nei-Hu Dist, Taipei, Taiwan, R.O.C.  
TEL:886-2-77188888 FAX:886-2-77218668

Title

05.CPU SKL-H : DDR4 CH-A

Size B

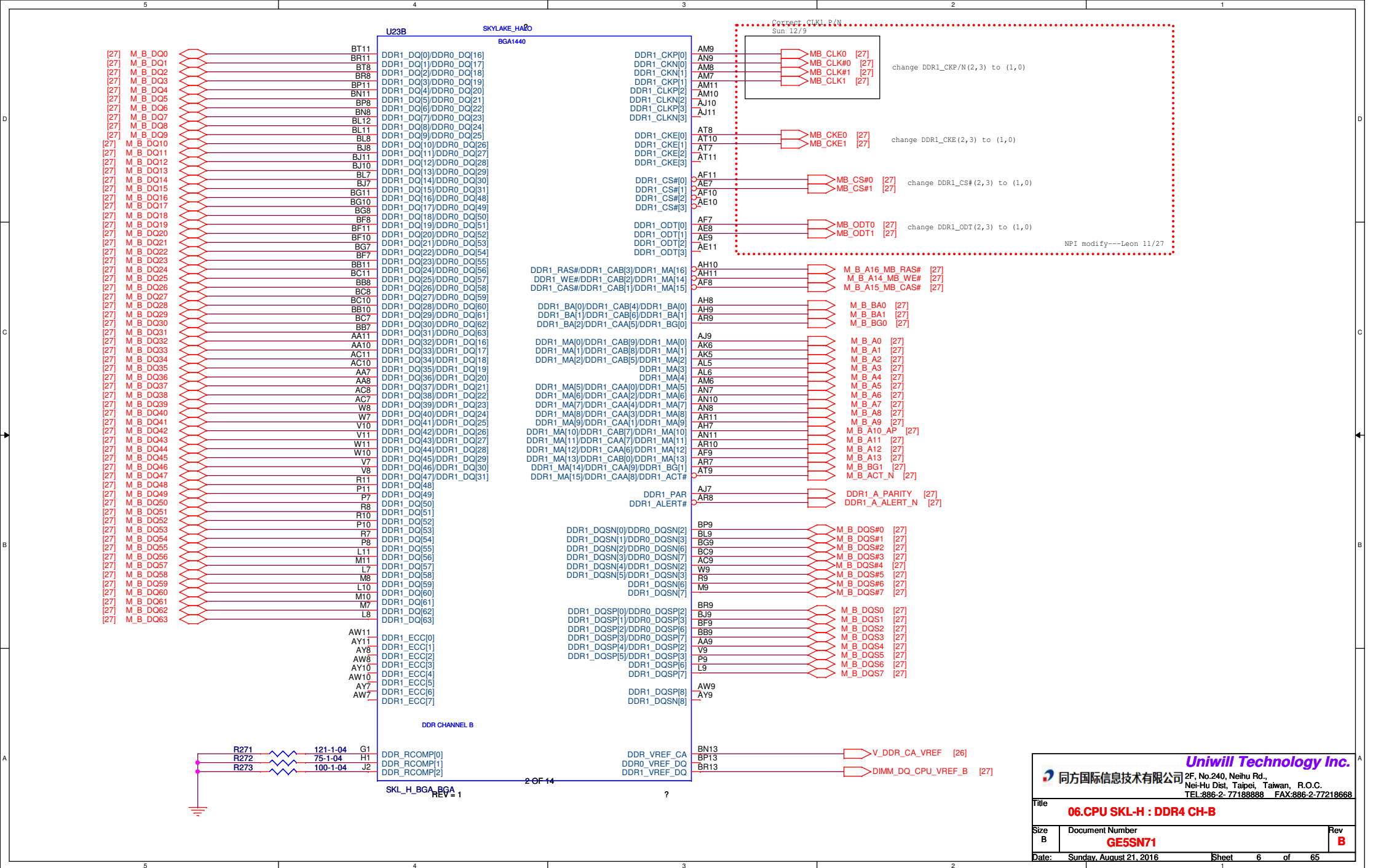
Document Number


GE5SN71

Rev B

Date: Sunday, August 21, 2016

Sheet 5 of 65



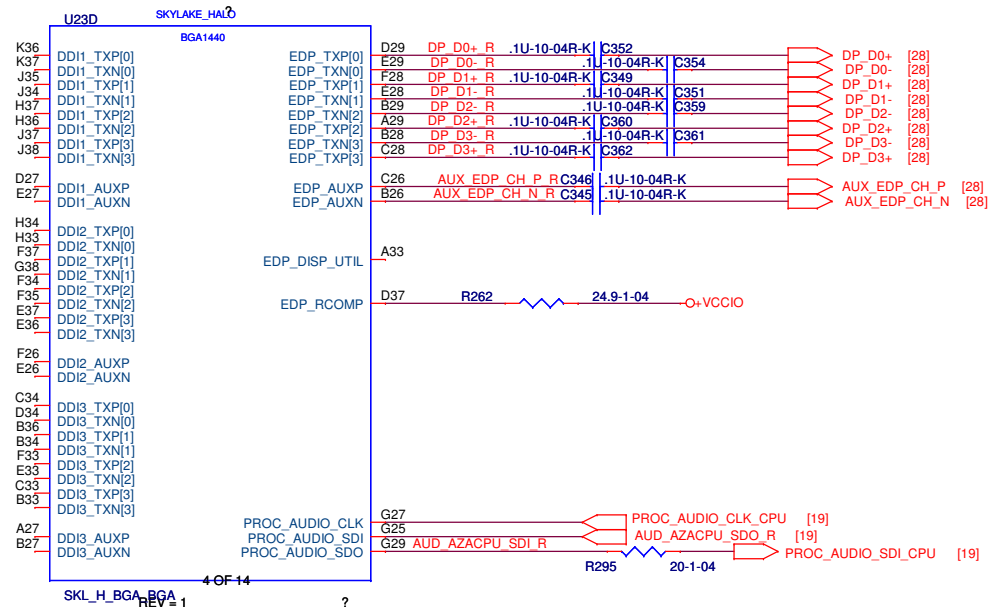
**Uniwill Technology Inc.**

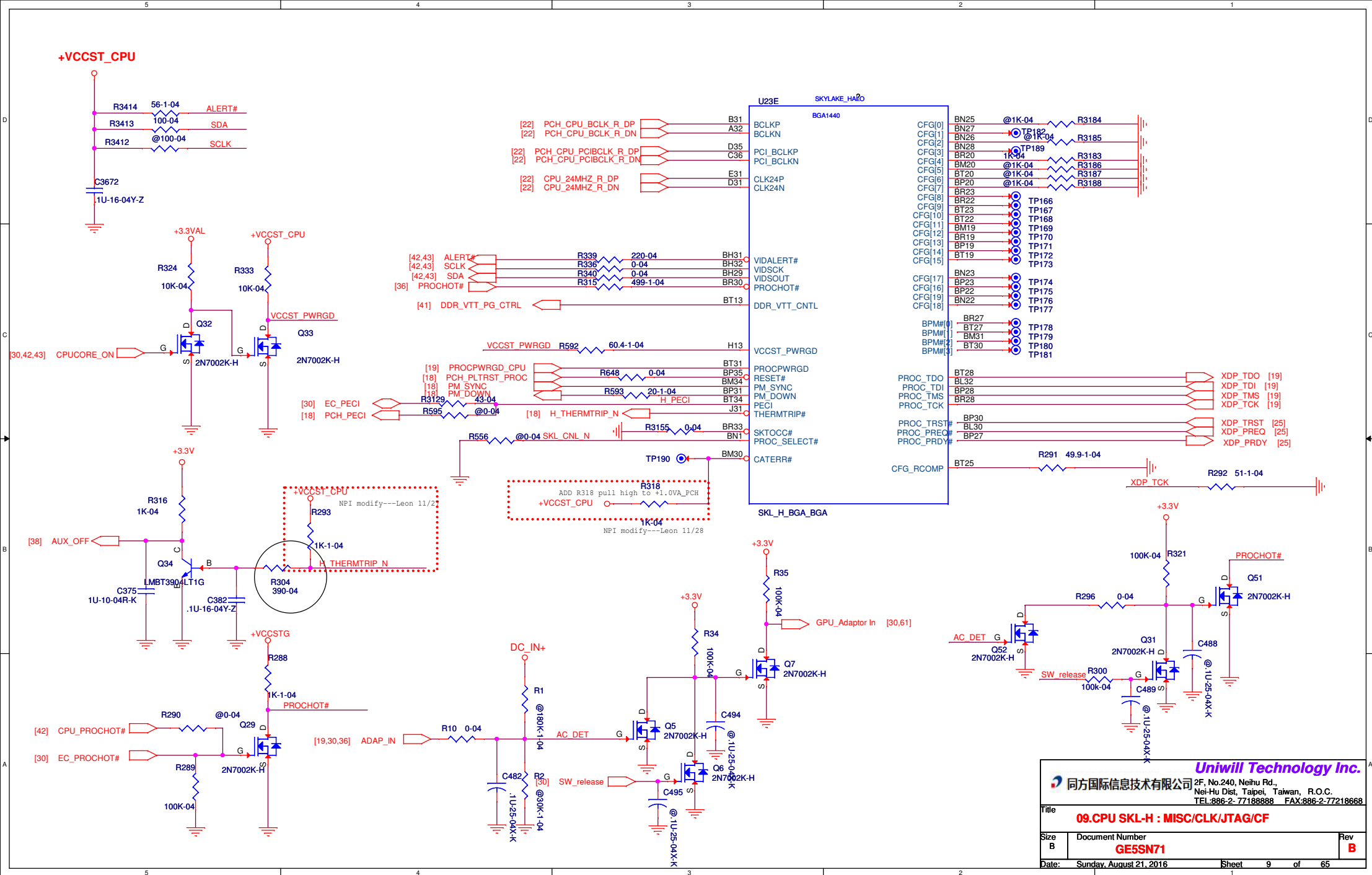
同方国际信息技术有限公司

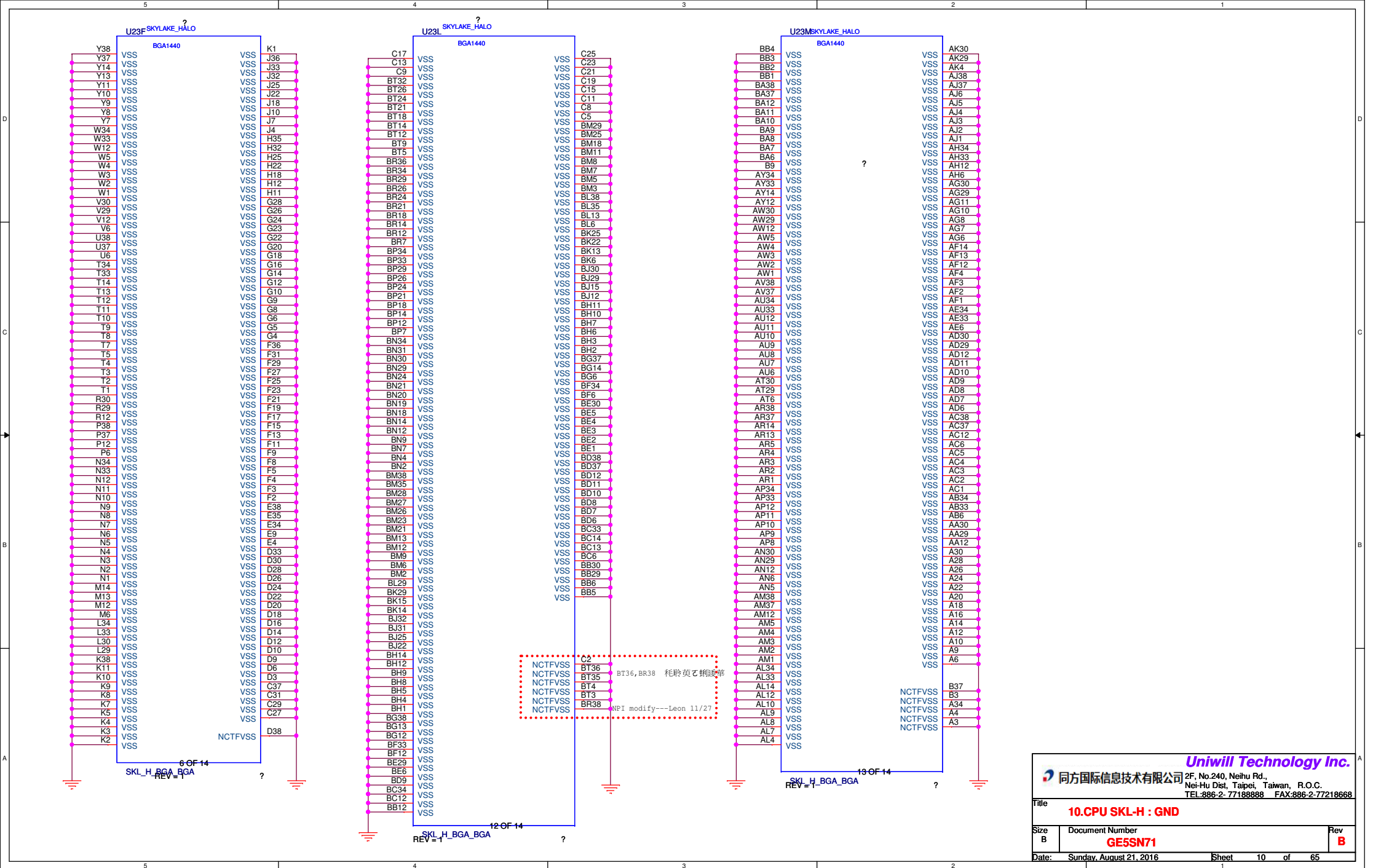
2F, No.240, NeiHu Rd.,  
Nei-Hu Dist, Taipei, Taiwan, R.O.C.  
TEL:886-2-77188888 FAX:886-2-77218668

Title		
06.CPU SKL-H : DDR4 CH-B		
Size	Document Number	Rev
B	GE5SN71	B
Date:	Sunday, August 21, 2016	Sheet 6 of 65





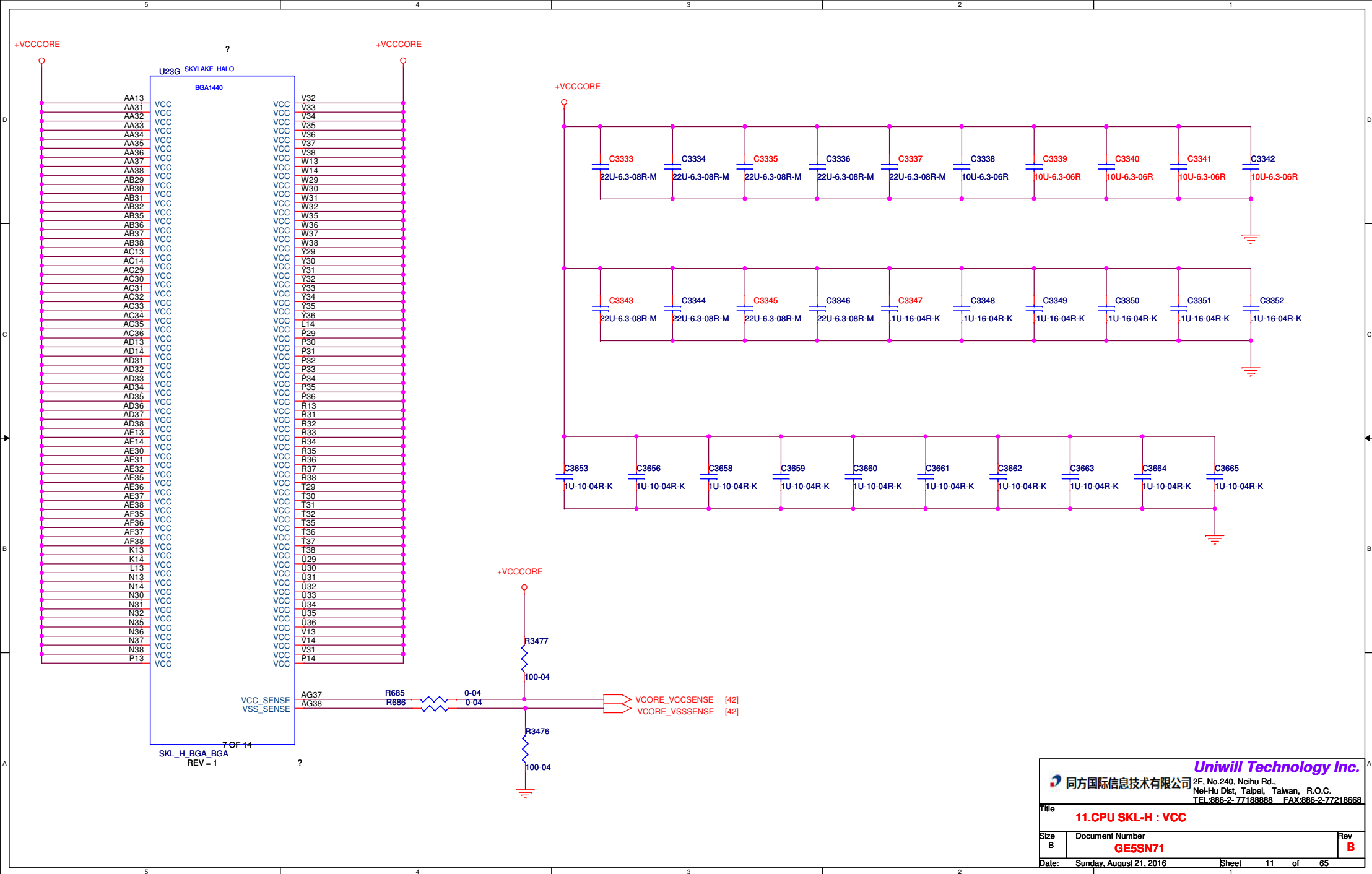


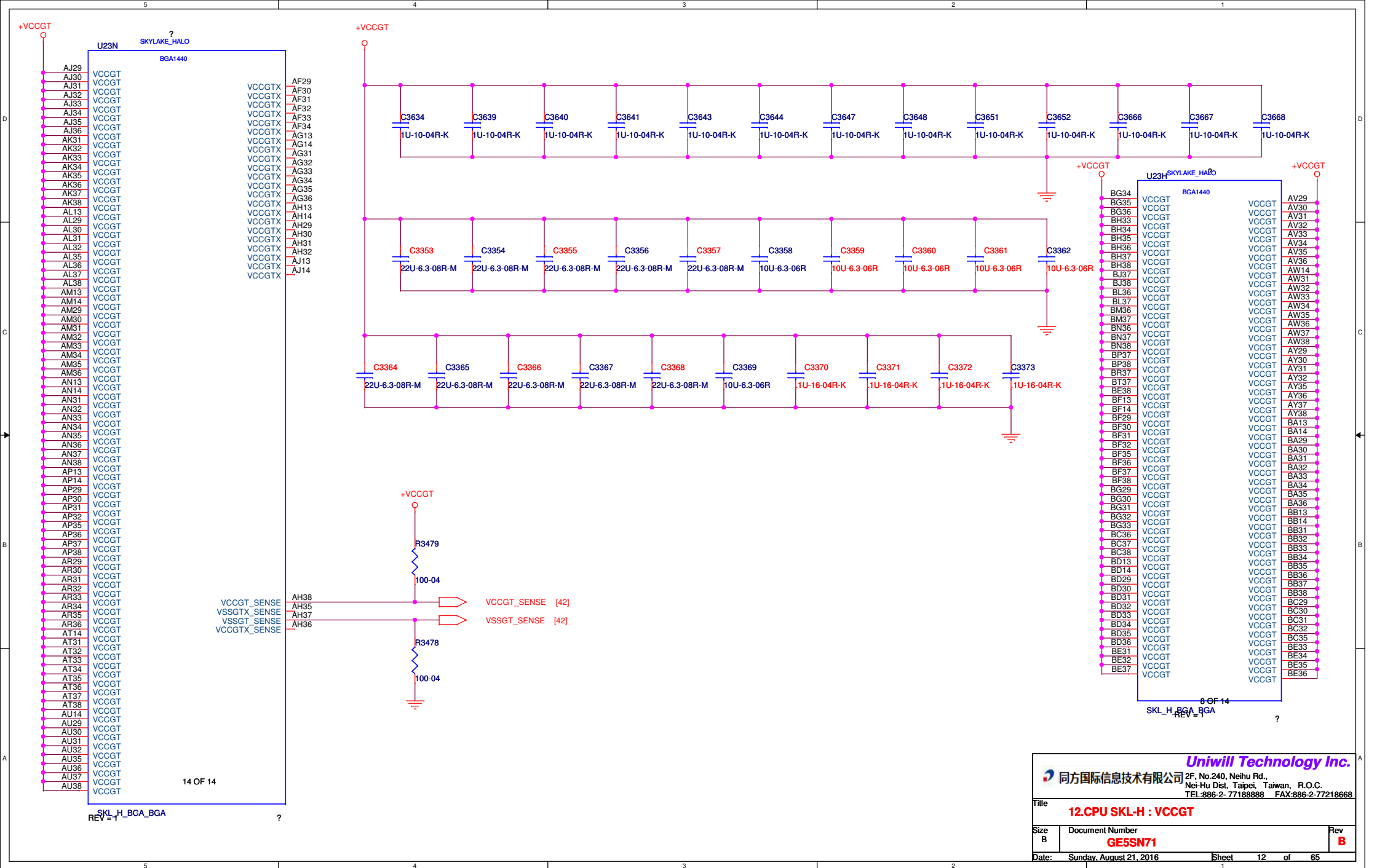


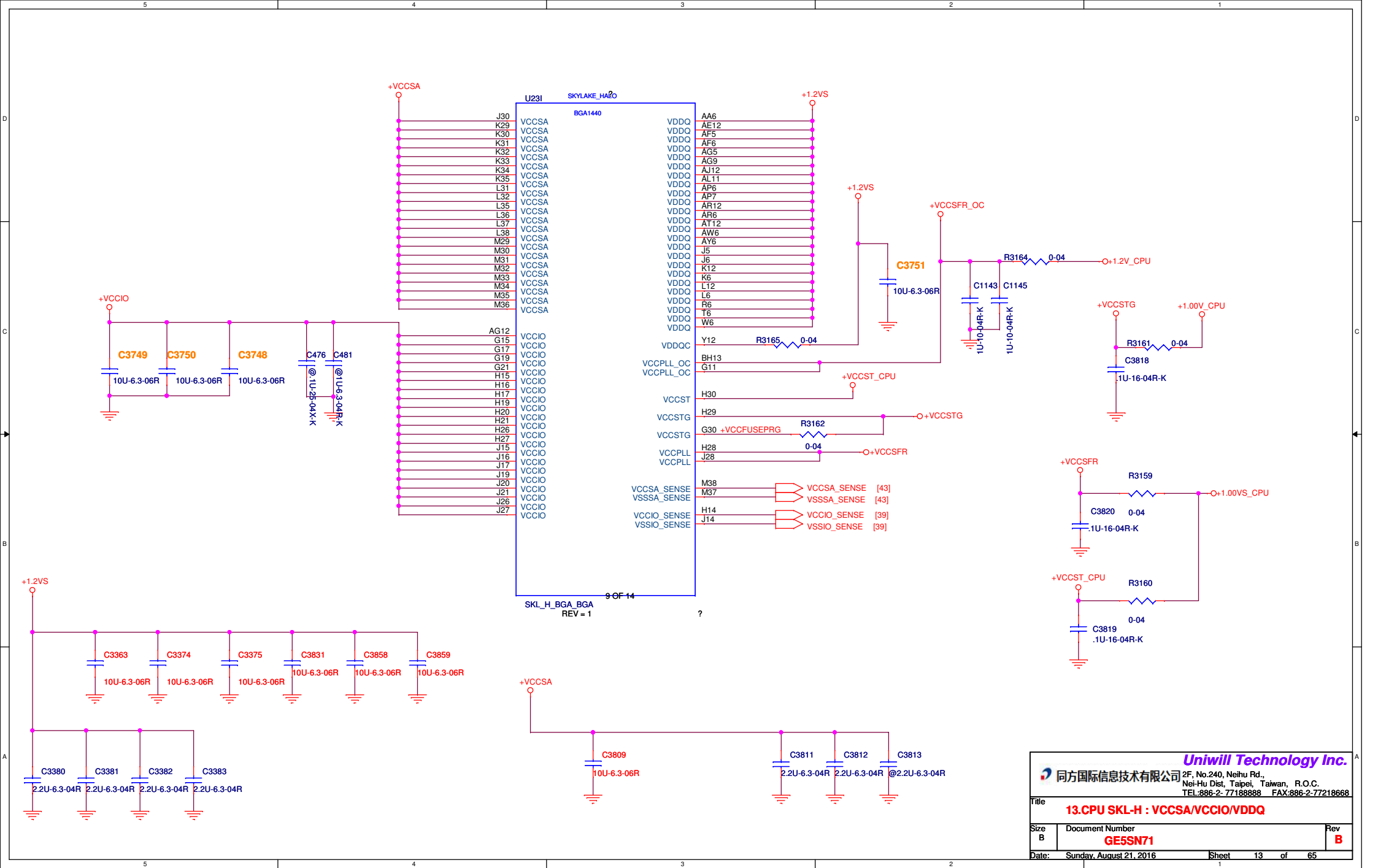
**Uniwill Technology Inc.**  
同方国际信息技术有限公司  
2F, No.240, Nei-Hu Rd.,  
Nei-Hu Dist, Taipei, Taiwan, R.O.C.  
TEL:886-2-77188888 FAX:886-2-77218668

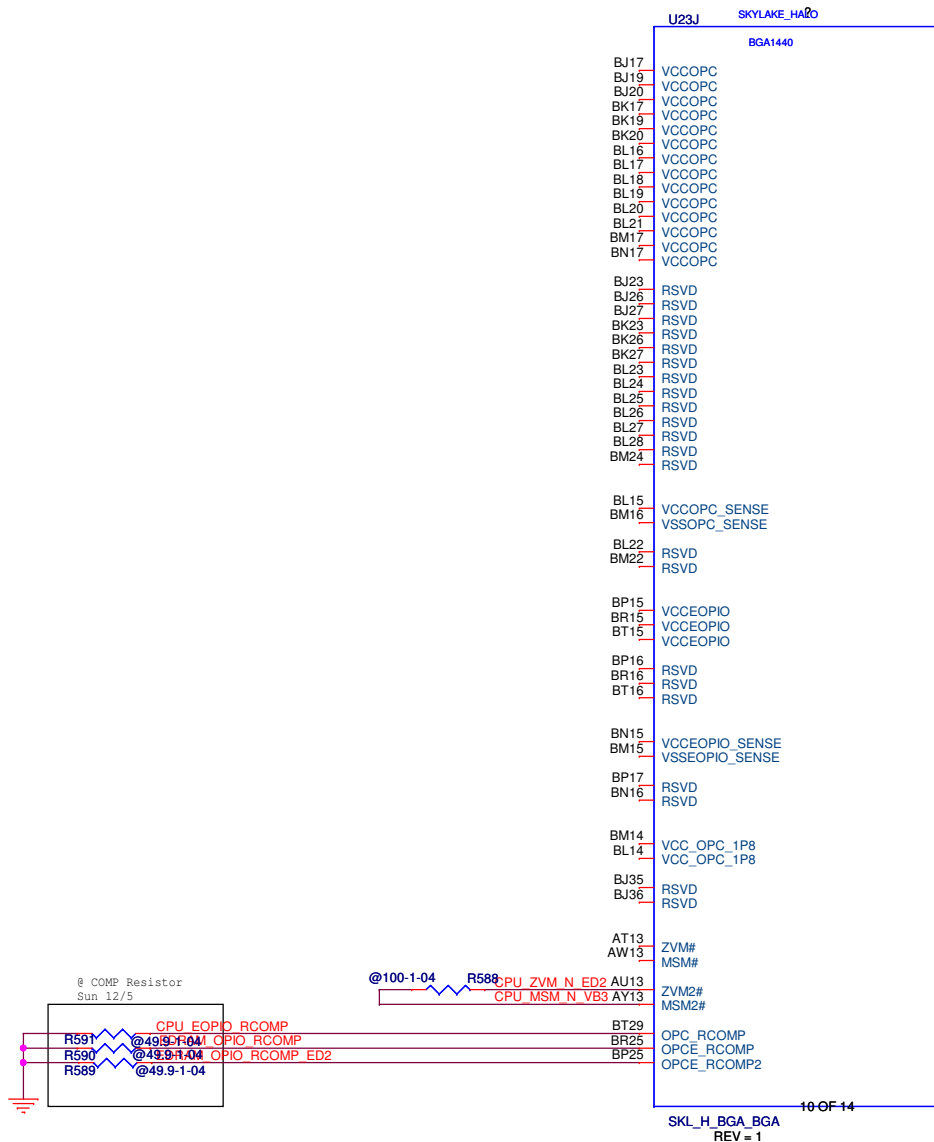
Title: **10.CPU SKL-H : GND**

Size B	Document Number <b>GE5SN71</b>	Rev <b>B</b>
Date: Sunday, August 21, 2016	Sheet 10	of 65



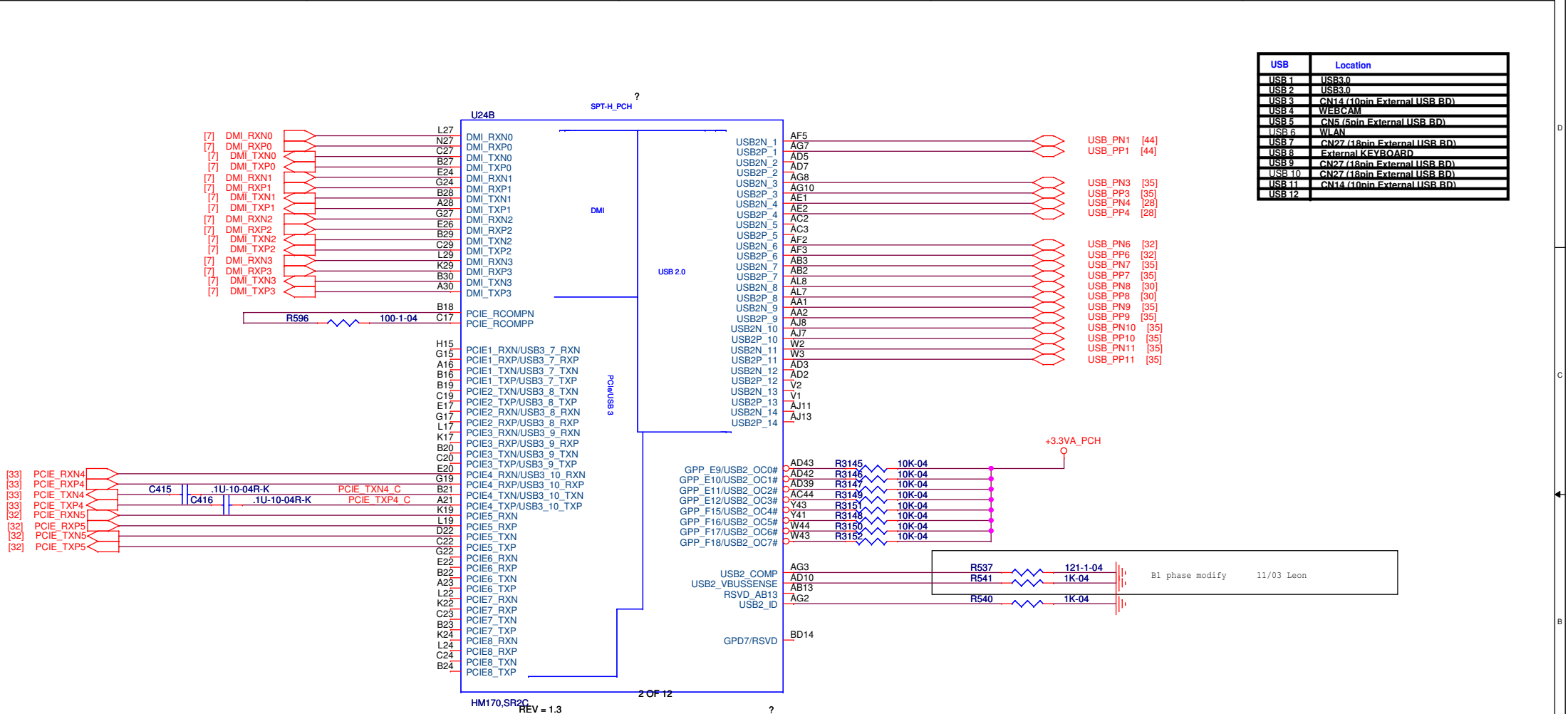






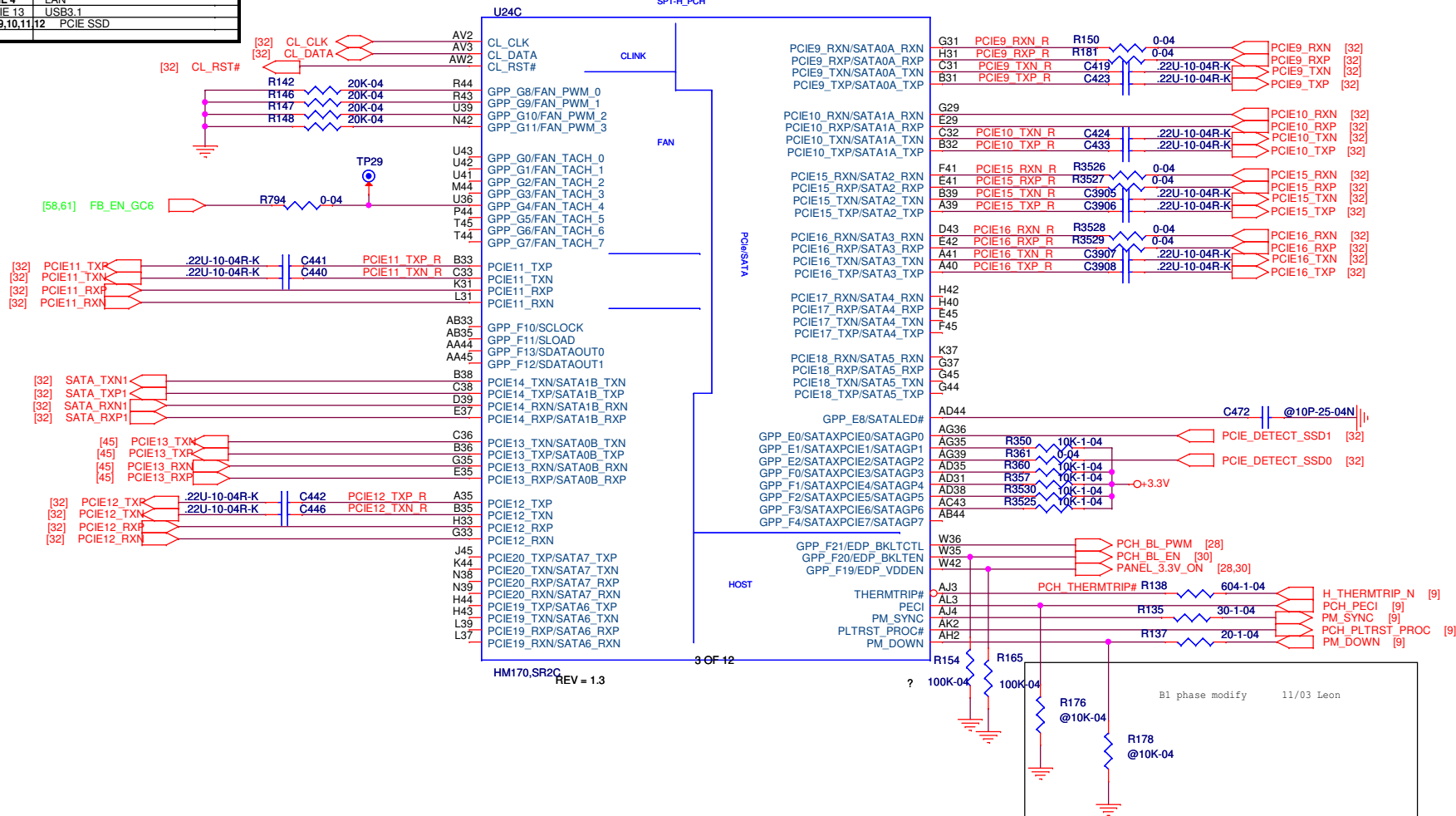






USB	Location
USB 1	USB3_0
USB 2	USB3_0
USB 3	CN14 (10pin External USB BD)
USB 4	WEBCAM
USB 5	CN5 (5pin External USB BD)
USB 6	WLAN
USB 7	CN27 (18pin External USB BD)
USB 8	External KEYBOARD
USB 9	CN27 (18pin External USB BD)
USB 10	CN27 (18pin External USB BD)
USB 11	CN14 (10pin External USB BD)
USB 12	

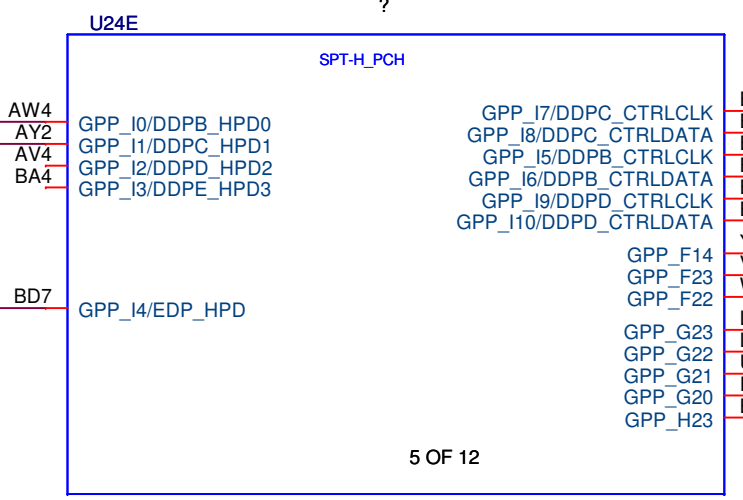
PCIE	Location
PCIE 16	SSD2(SATA)
PCIE 5	WLAN
PCIE 15	SATA
PCIE 9	SSD1(SATA)
PCIE 4	LAN
PCIE 13	USB3.1
PCIE 9,10,11	PCIE SSD





[29,30] HDMI\_HPD  
[29,30] DP\_HPD

[28] EDP\_HPD




BB3  
BD6  
BA5  
BC4  
BE5  
BE6  
Y44  
V44  
W39  
L43  
L44  
U35  
R35  
BD36

Boost FAN\_EN [35]  
Boost FAN\_EN1 [35]

5 OF 12

HM170,SR2C  
REV = 1.3



同方国际信息技术有限公司

2F, No.240, NeiHu Rd.,  
Nei-Hu Dist, Taipei, Taiwan, R.O.C.  
TEL:886-2- 77188888 FAX:886-2-77218668

Title

20.PCH SKL-H : DDI CONTROL

Size  
A

Document Number  
GE5SN71

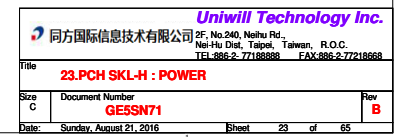
Rev  
B

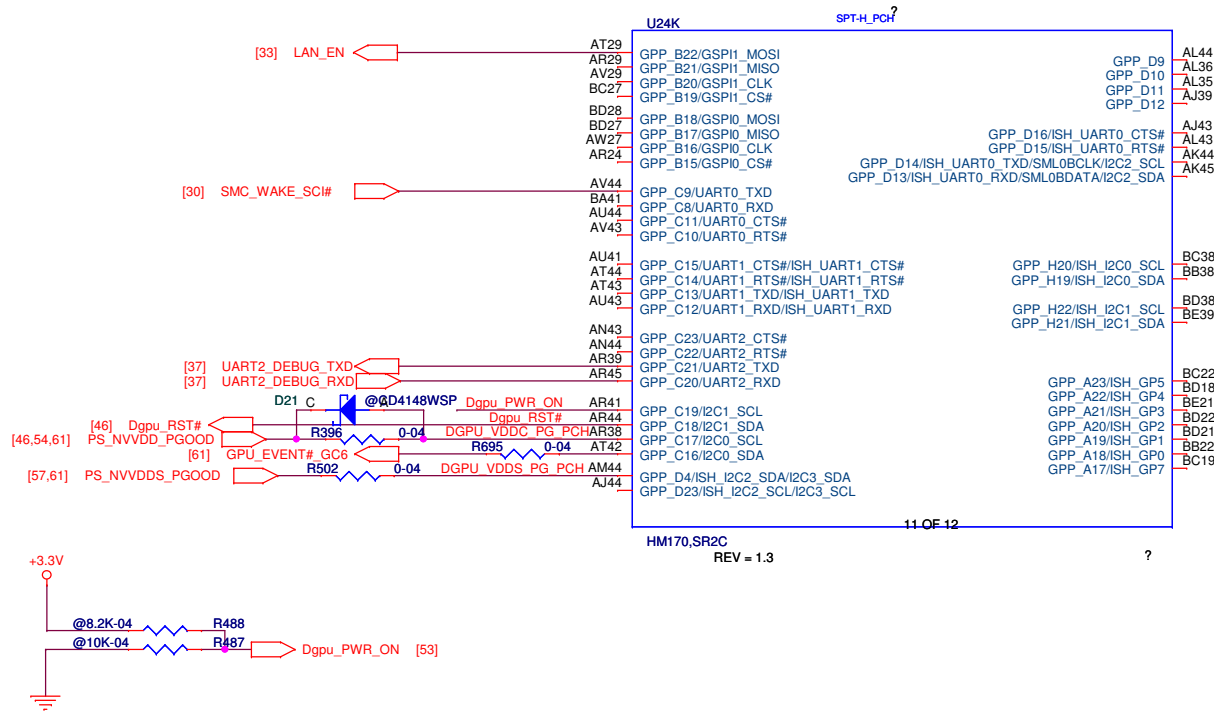
Date: Sunday, August 21, 2016

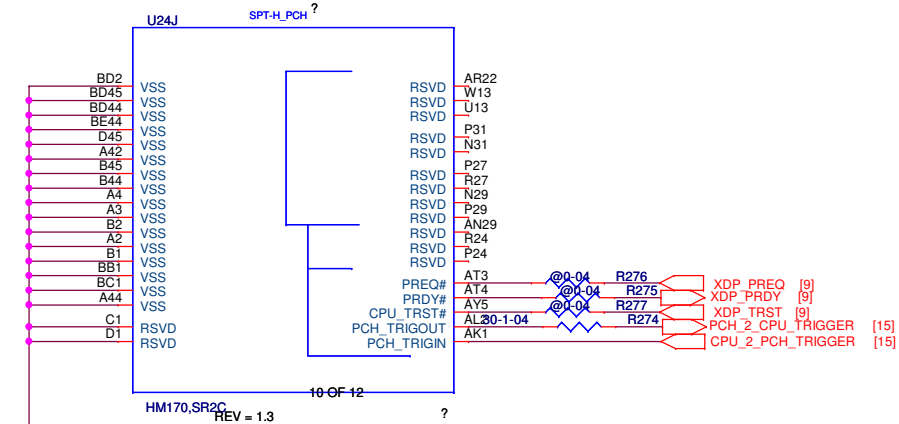
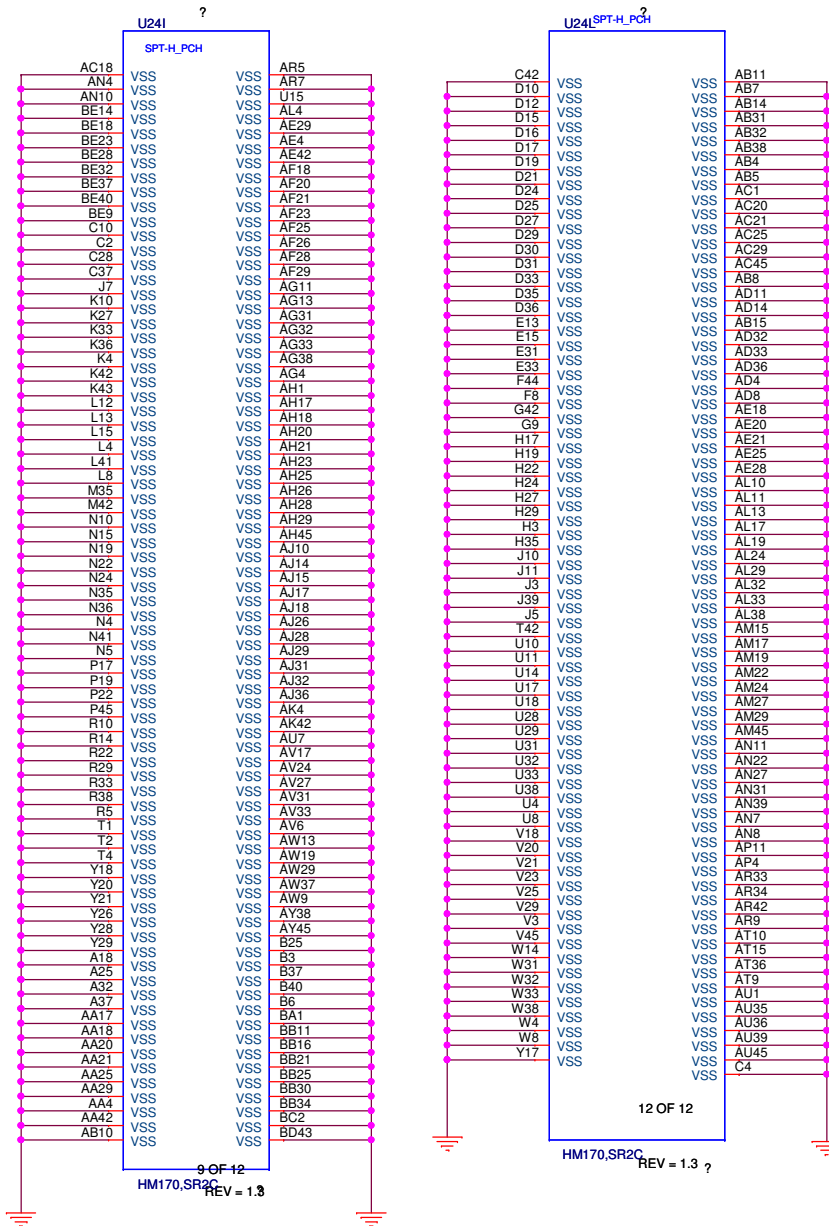
Sheet 20 of 65



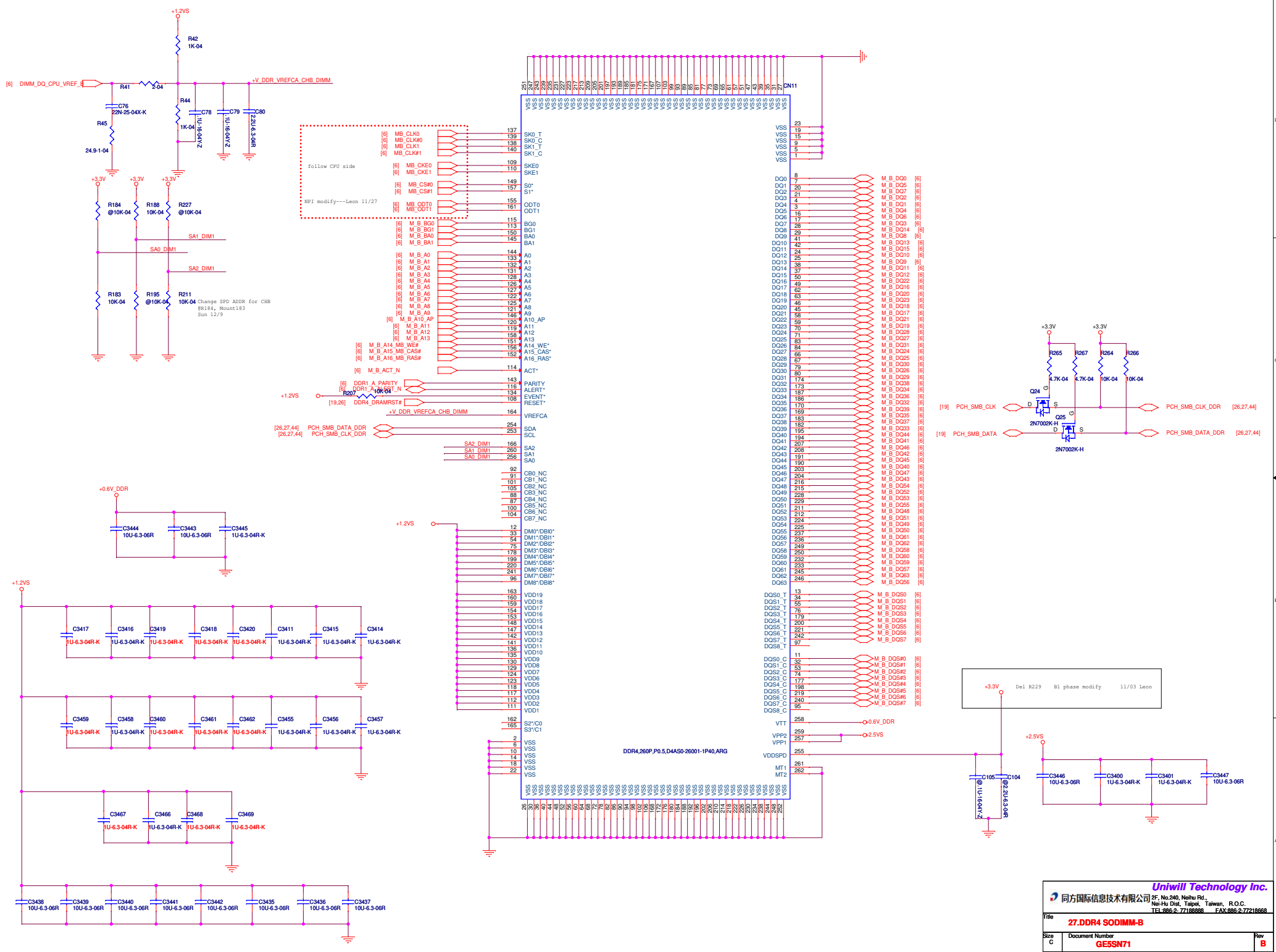


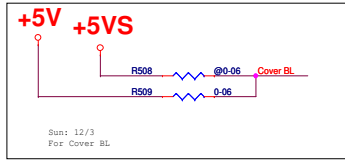
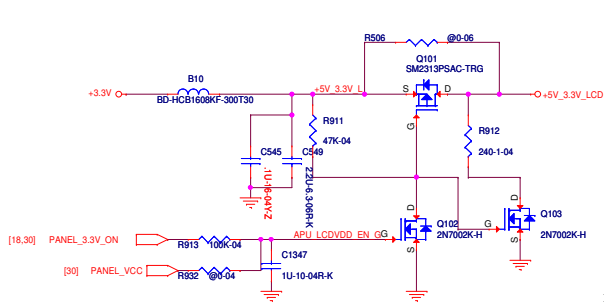




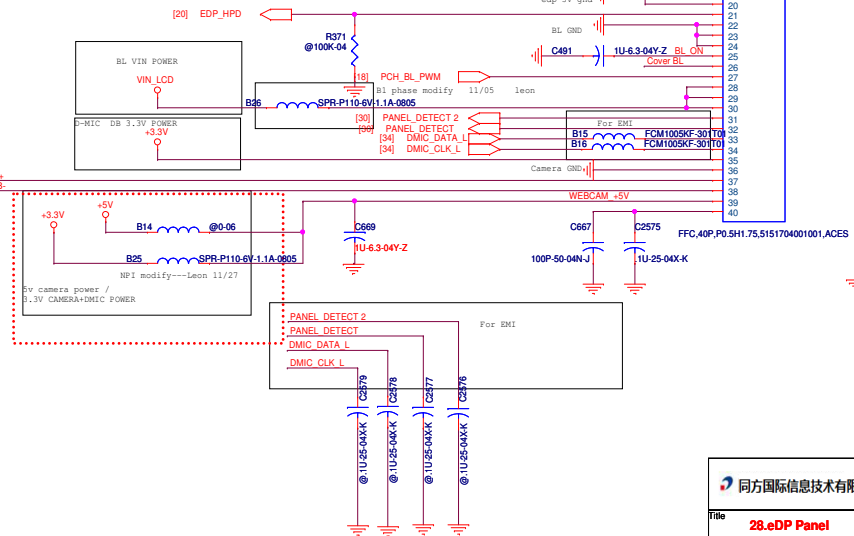
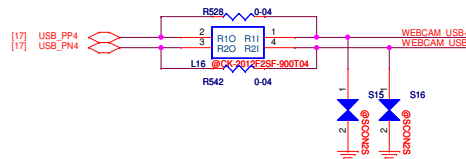
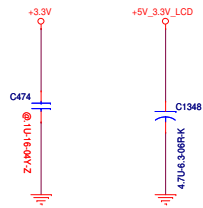
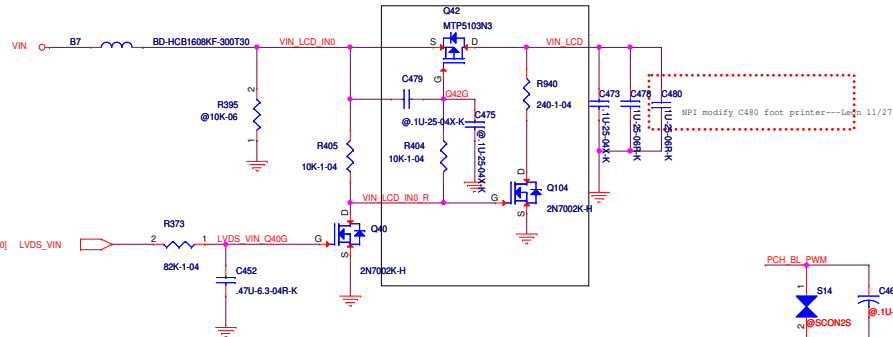
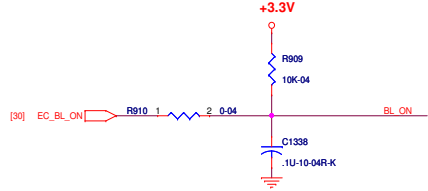
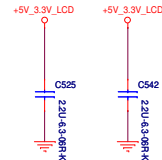




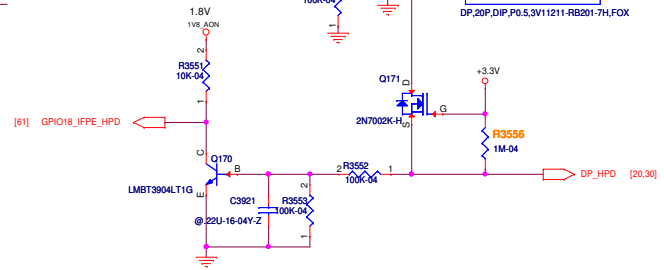
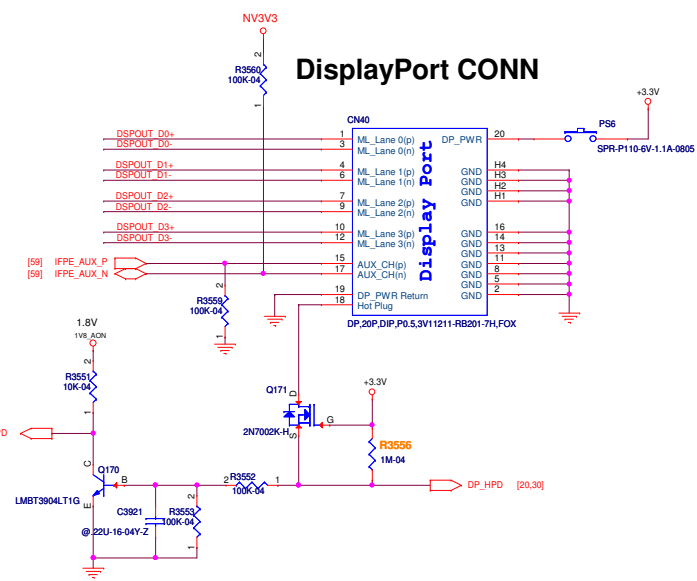




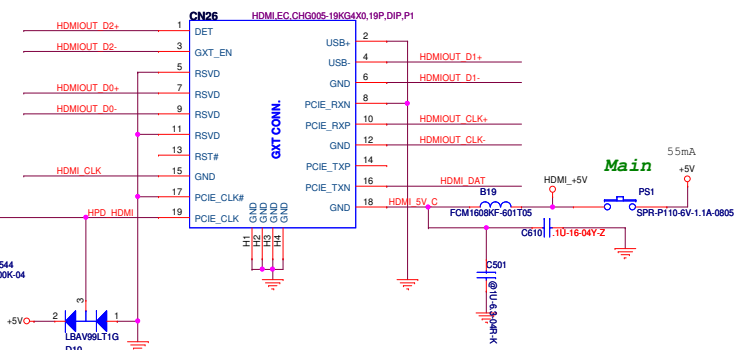
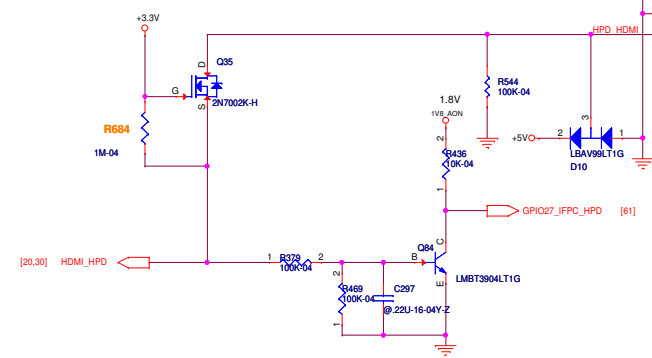
For 14" & 15" B10上件 B9 OP



Panel_det	14"	15"	18"	23"
PANEL_DETECT	1	0	1	0
PANEL_DETECT2	1	1	0	0



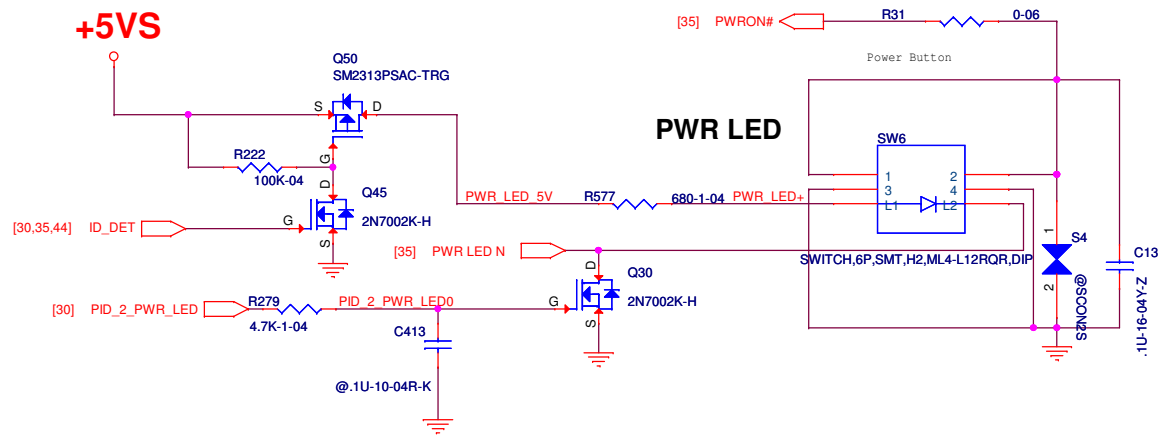
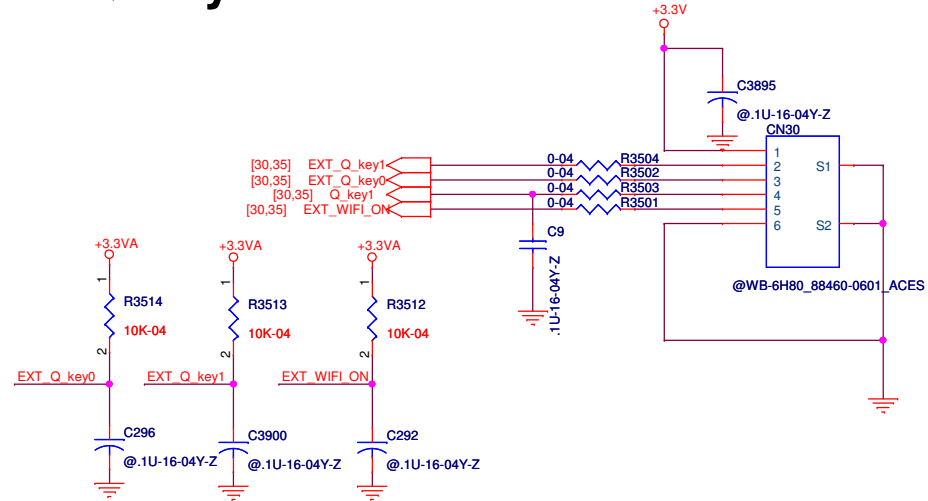
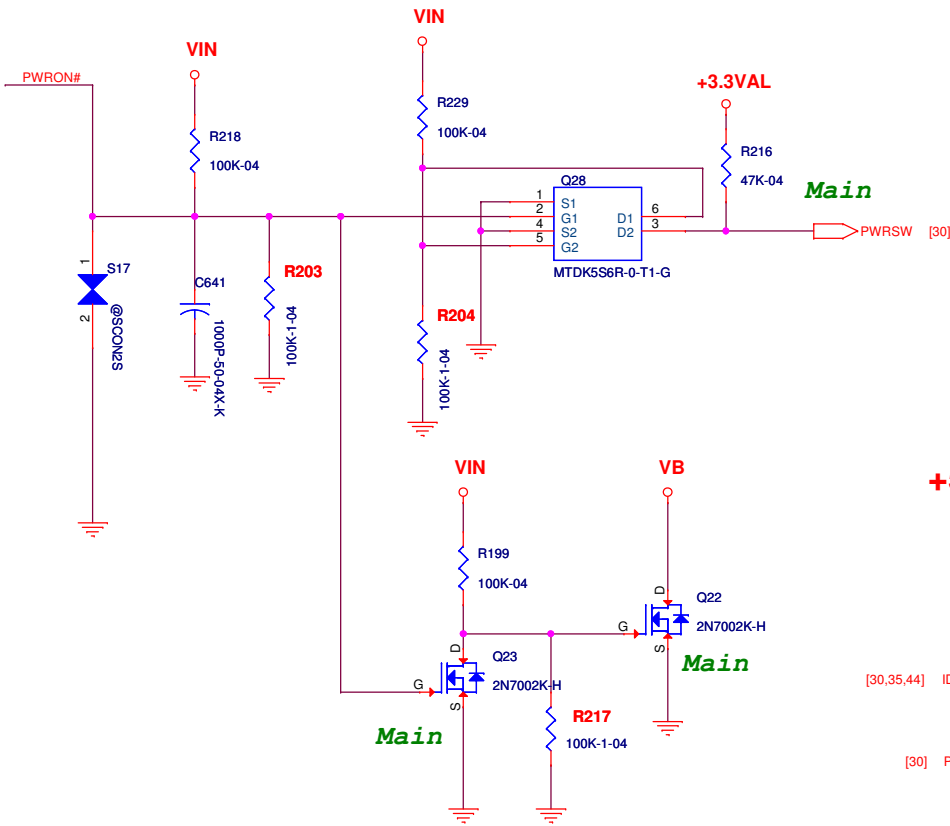
## HDMI CONN



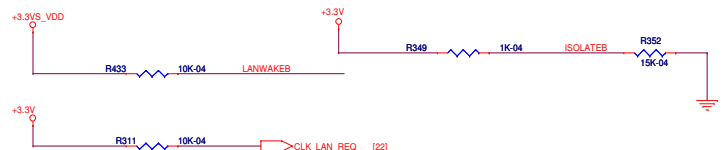


PWR SW

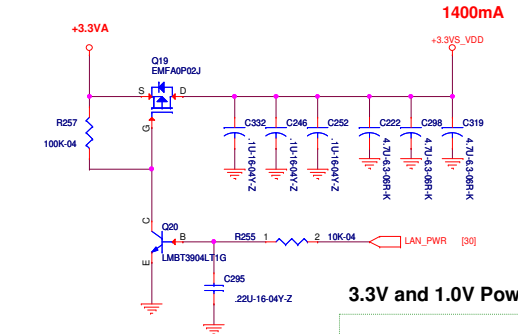
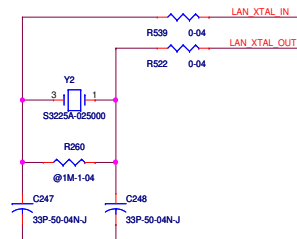
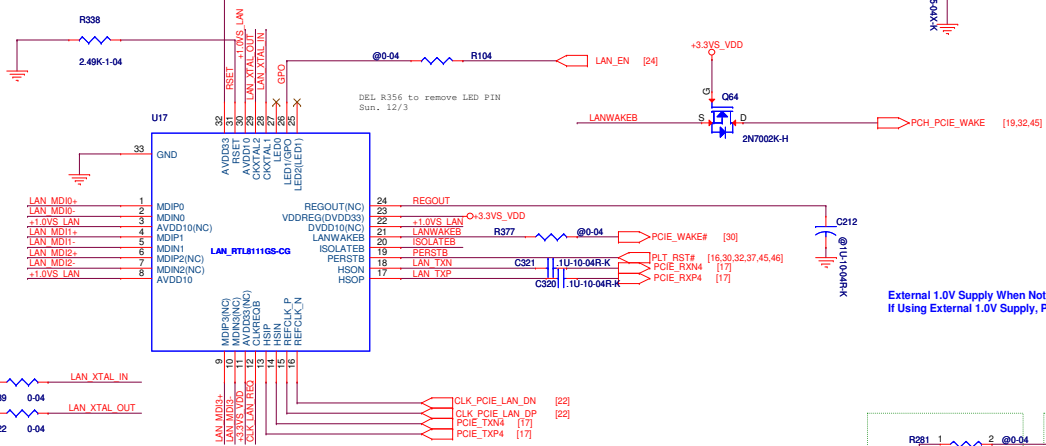
Q Key







RTL8118A(S)  
LAN IC



### 3.3V and 1.0V Power-Supply Configurations

	1.0 V source	Lx	Cou1,2	Cin1,2	R1	C7
RTL8111G Series/ RTL8111H Series/ RTL8107E Series	LDO	X	X	X	O	O
RTL8111G Series/ RTL8111H Series/ RTL8107E Series	External	X	X	X	X	O
RTL8111GS Series/ RTL8111GUS Series/ RTL8111HS Series/ RTL8106EUS Series/ RTL8107ES Series/ RTL8118AS Series	SWR	O	O	O	X	X
RTL8106E Series	LDO	X	X	X	X	X

Note:

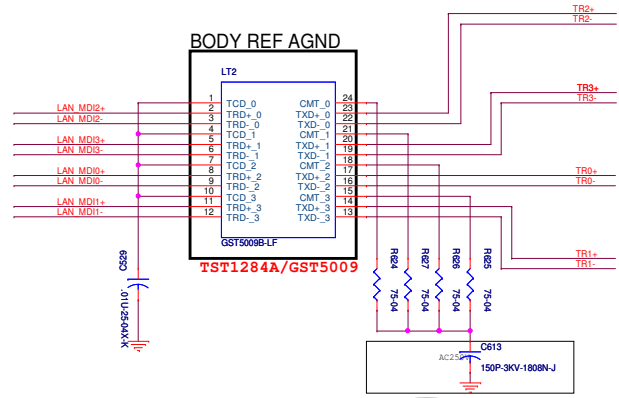
1. R1 is reserved for the convenience of changing the 1.0V supply source between SWR/LDO mode and external supply. No design change of PCB model is needed with R1 reserved.

If only one 1.0V supply source is selected for one PCB model, i.e. no other choices are reserved:

a. For RTL8111G Series, RTL8111H Series and RTL8107E Series, LDO mode only

2. Please refer to the table above when using different 1.0V supply source.

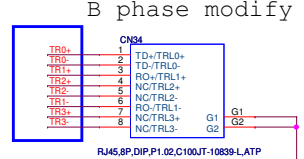
a. For RTL8111GS Series, RTL8111GUS Series, RTL8111HS Series, RTL8106E Series, RTL8106EUS Series, RTL8107ES Series and RTL8118AS Series, External 1.0V Supply is Not Permitted.



BODY REF AGND  
LT2  
TST1284A/GST5009

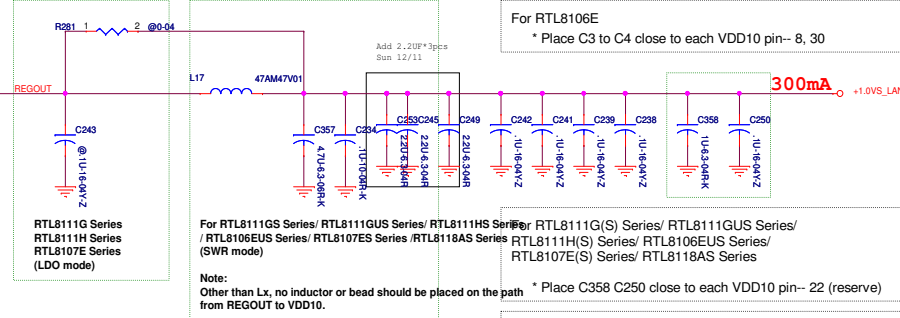
Delete RJ45 w/LED PIN  
Sun. 12/3

External 1.0V Supply When Not Using SWR/LDO mode for RTL8111G(S).  
If Using External 1.0V Supply, Pls. Contact With FAE.



For RTL8111G(S)  
\* Place C3 to C6 close to each VDD10 pin-- 3, 8, 22, 30

For RTL8106E  
\* Place C3 to C4 close to each VDD10 pin-- 8, 30



For RTL8111GS Series/ RTL8111GUS Series/ RTL8111HS Series/ RTL8111GUS Series/ RTL8111H Series/ RTL8106EUS Series/ RTL8107ES Series/ RTL8118AS Series

Note:  
Other than Lx, no inductor or bead should be placed on the path from REGOUT to VDD10.

For RTL8106E  
\* Place C358 C250 close to each VDD10 pin-- 30 (reserve)

**AMP VDD**



# FAN CONTROLLER

The schematic diagram illustrates a Fan Controller circuit, divided into four main sections: FAN, CPU FAN, GPU FAN, and SYS FAN. Each section includes a boost driver (U87, U88, U724), a MOSFET (Q10, Q11, Q15, Q12), and a fan motor. The boost drivers are configured as push-pull stages. The MOSFETs are driven by the boost drivers. The fan motors are connected to the MOSFETs. The circuit also includes a temperature sensor (Q111) and a temperature controller (U14). The temperature controller is configured to control the fan speed based on the temperature of the CPU. The circuit is powered by a 5V supply and includes various passive components (resistors, capacitors).

**FAN Section:** Includes U87 (MP2314GJ.MPS.TSOT23-8), Q10 (SM2313PSAC-TRG), Q111 (2N7002K-H), and U14 (APL5607AKI-TRG). It features a boost driver (U87) and a MOSFET (Q10) driving a fan motor. A temperature sensor (Q111) and a temperature controller (U14) are also present.

**CPU FAN Section:** Includes U88 (MP2314GJ.MPS.TSOT23-8), Q15 (SM2313PSAC-TRG), Q12 (2N7002K-H), and U724 (MP2314GJ.MPS.TSOT23-8). It features a boost driver (U88) and a MOSFET (Q15) driving a fan motor. A temperature sensor (Q12) and a temperature controller (U724) are also present.

**GPU FAN Section:** Includes U724 (MP2314GJ.MPS.TSOT23-8), Q12 (2N7002K-H), Q15 (SM2313PSAC-TRG), and U88 (MP2314GJ.MPS.TSOT23-8). It features a boost driver (U724) and a MOSFET (Q12) driving a fan motor. A temperature sensor (Q15) and a temperature controller (U88) are also present.

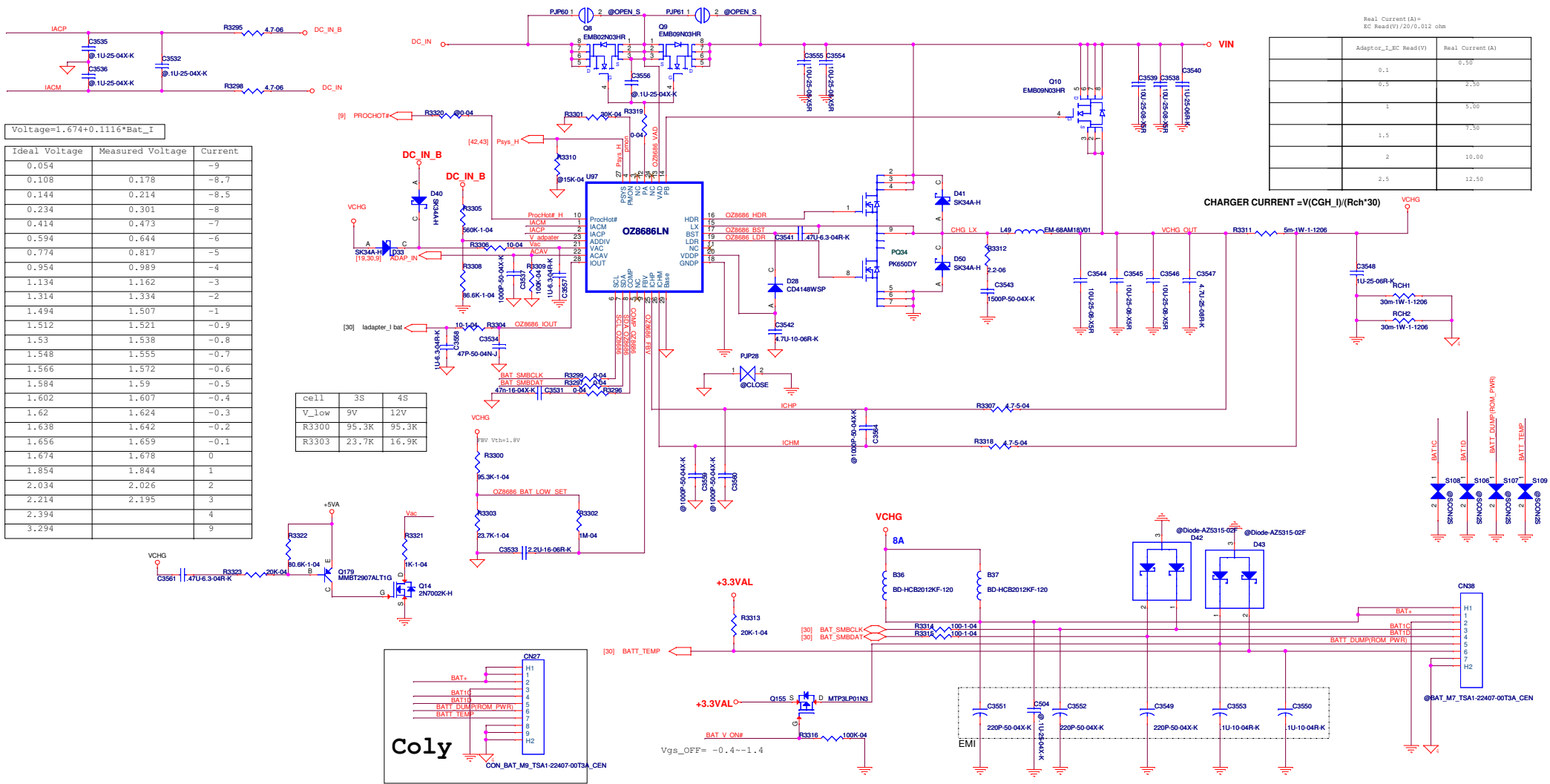
**SYS FAN Section:** Includes U724 (MP2314GJ.MPS.TSOT23-8), Q12 (2N7002K-H), Q15 (SM2313PSAC-TRG), and U88 (MP2314GJ.MPS.TSOT23-8). It features a boost driver (U724) and a MOSFET (Q12) driving a fan motor. A temperature sensor (Q15) and a temperature controller (U88) are also present.

**Temperature Sensor and Controller:** The temperature sensor (Q111) is connected to the temperature controller (U14). The temperature controller (U14) is configured to control the fan speed based on the temperature of the CPU.

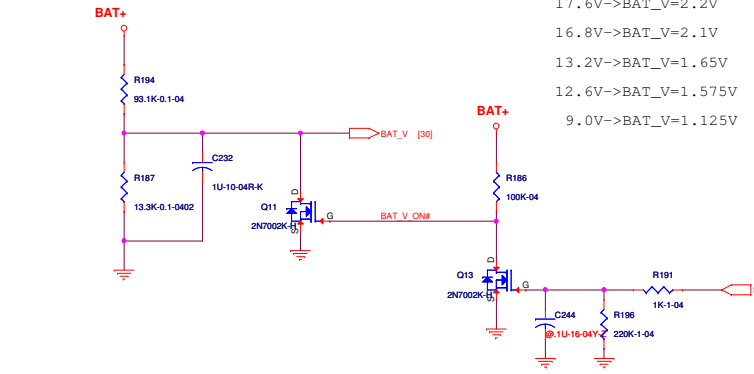
**Power and Grounding:** The circuit is powered by a 5V supply. Various passive components (resistors, capacitors) are used for signal conditioning and power filtering.

**Legend:** The legend defines the symbols used in the schematic, including components like U87, U88, U724, Q10, Q11, Q15, Q12, U14, and various resistors and capacitors.

**Uniwill Technology Inc. Information:** Uniwill Technology Inc. is located at 2F, No.240, Naihui Rd., Nei-Hu Dist., Taipei, R.O.C. TEL: 886-2-7718888 FAX: 886-2-7721888. The document is titled "35.EXT\_MIC/USB/FANG-sen" and is dated Sunday, August 21, 2018.



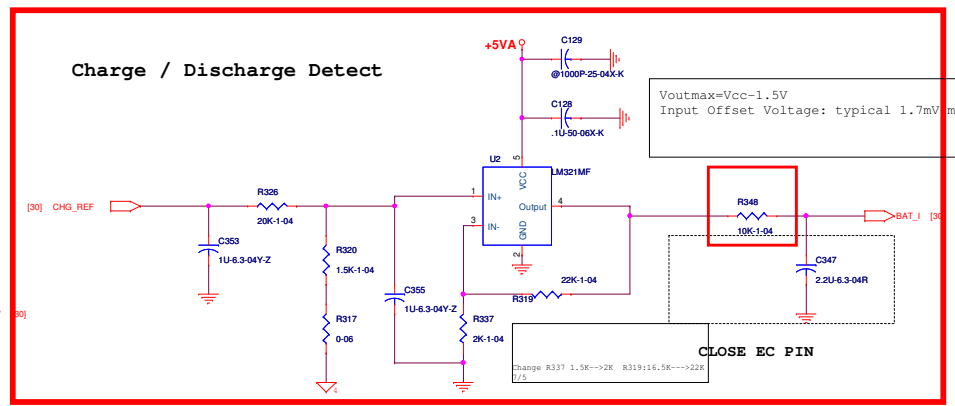
# Battery Voltage Detect



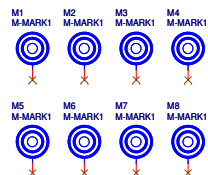
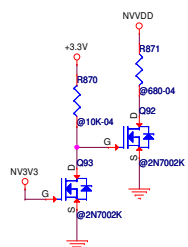
17.6V->BAT\_V=2.2V  
 16.8V->BAT\_V=2.1V  
 13.2V->BAT\_V=1.65V  
 12.6V->BAT\_V=1.575V  
 9.0V->BAT\_V=1.125V

6/12

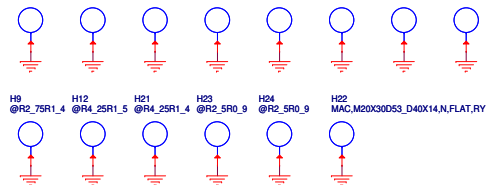
# Charge / Discharge Detect



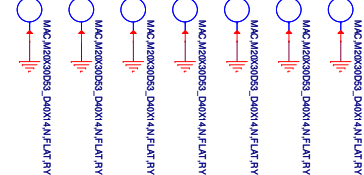
CN42  
DCIN WO 2DC3003-002211 SIN



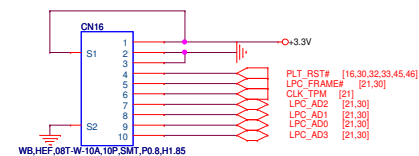
H2 H3 H4 H5 H6 H7 H8 H25



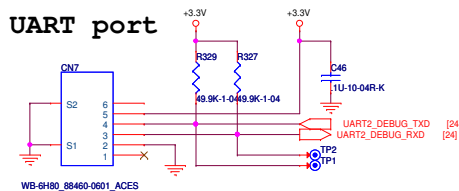
H13	H14	H15	H16	H18	H19	H20



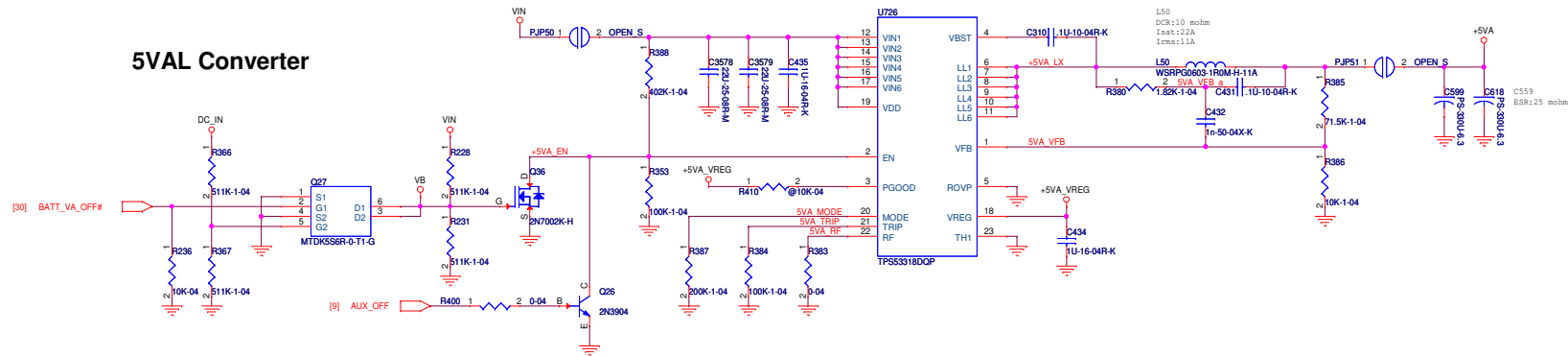
LPC port



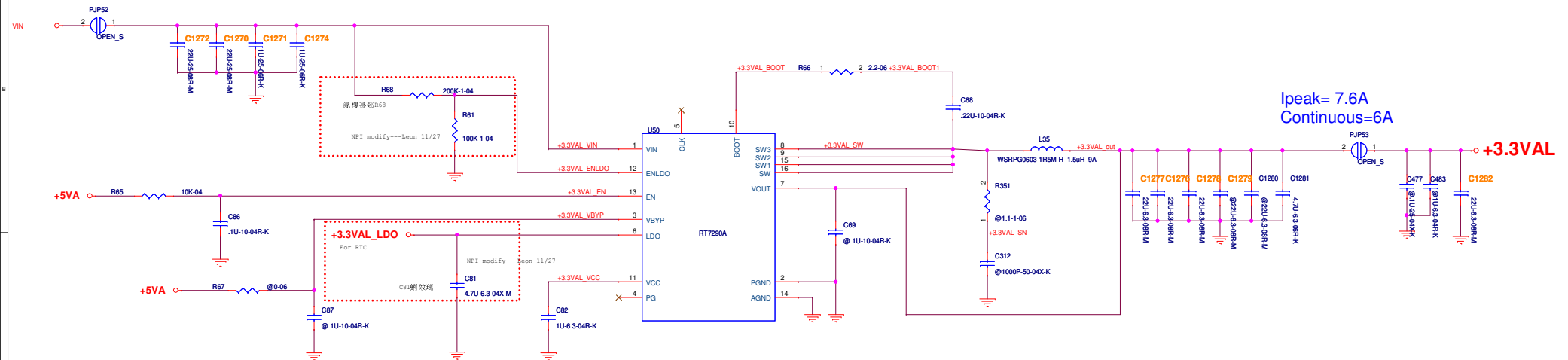
## UART port



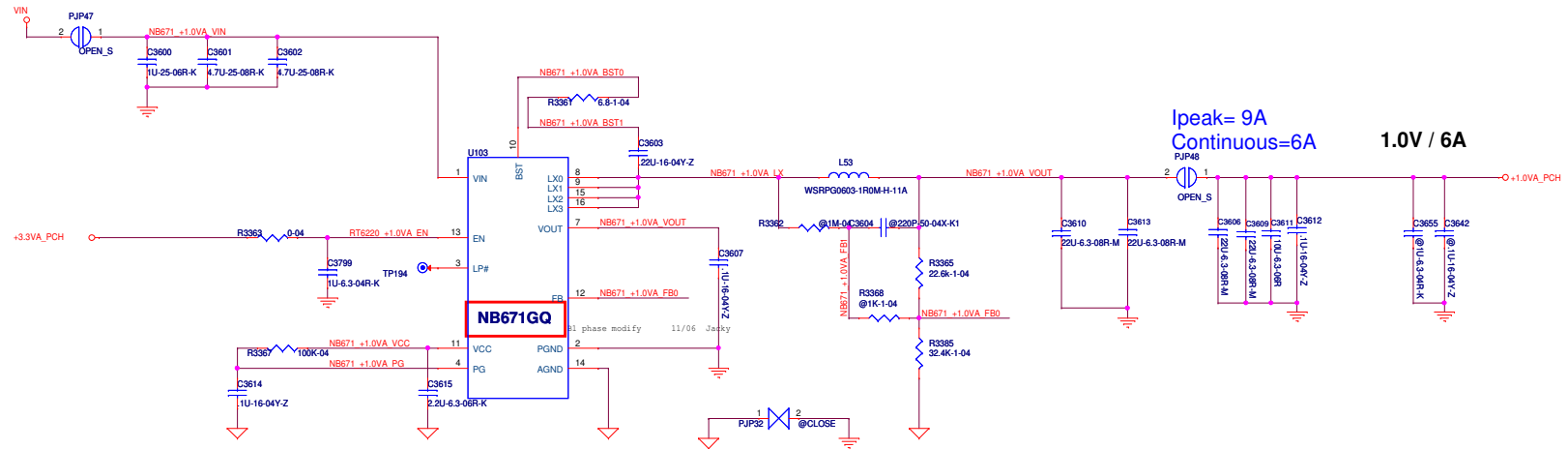
## 5VAL Converter



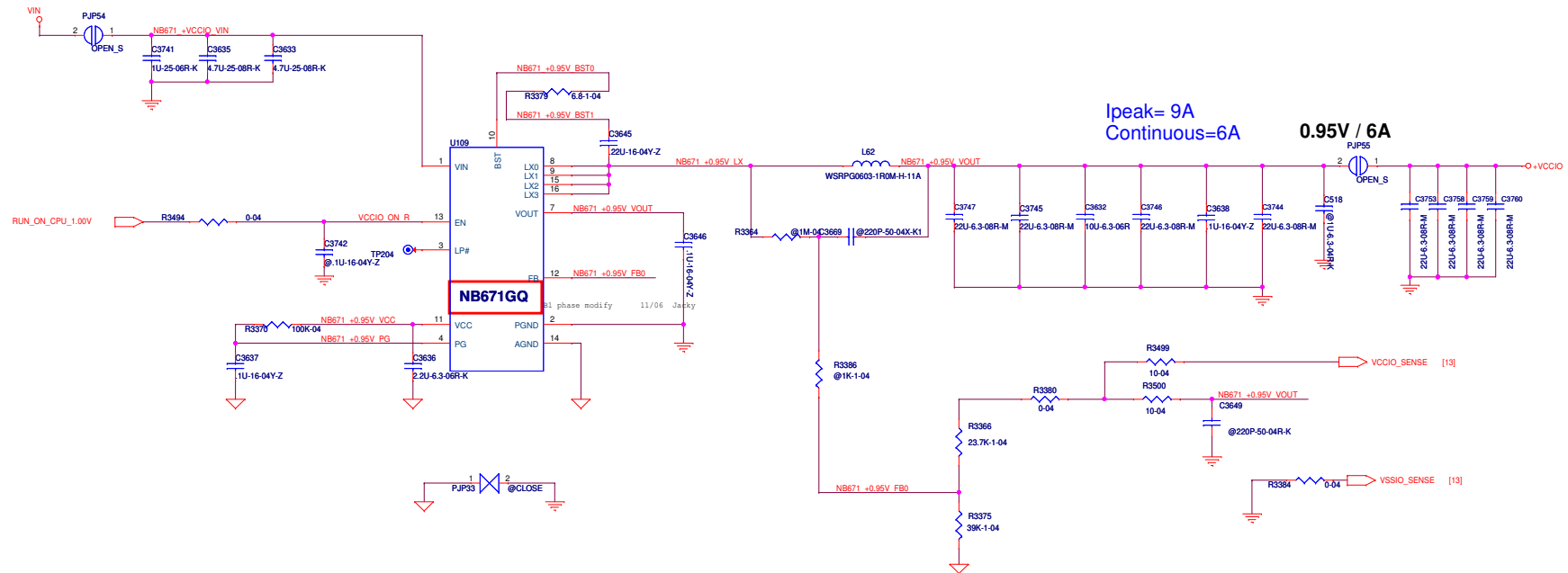
## 3.3VAL Converter



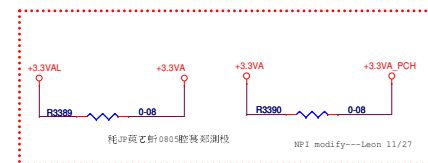
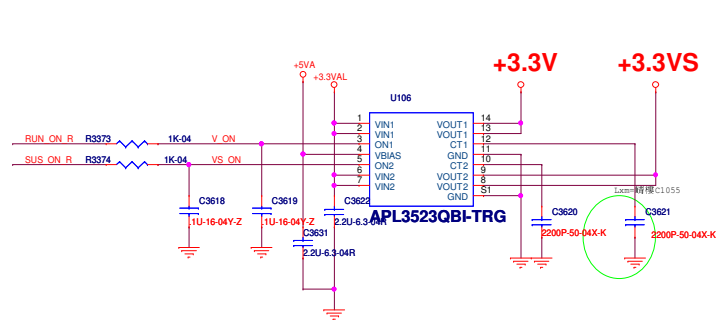
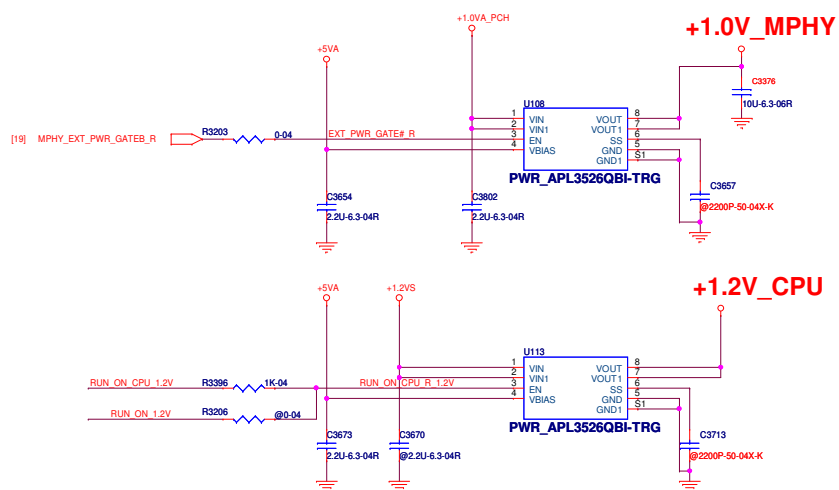
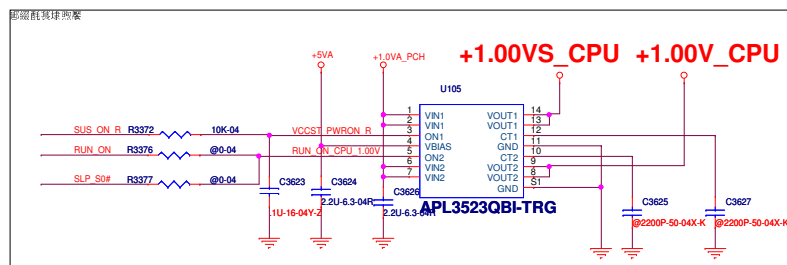
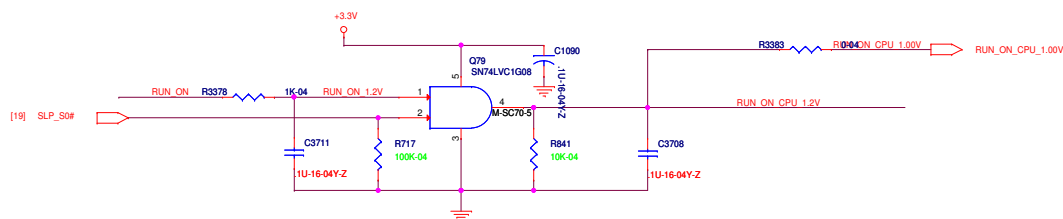
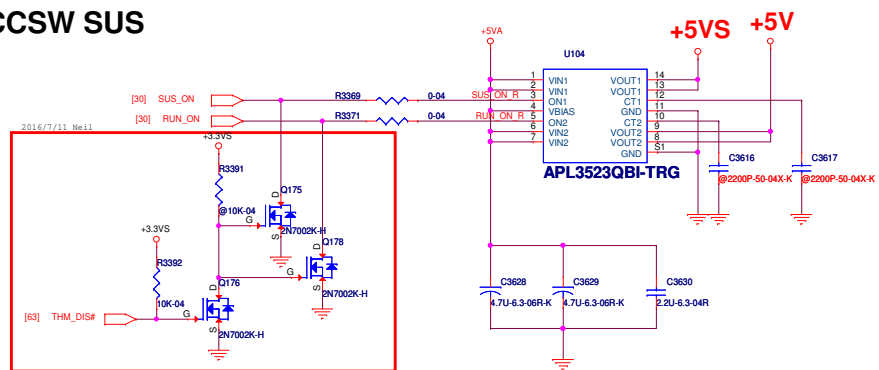
## 1.0VA Converter



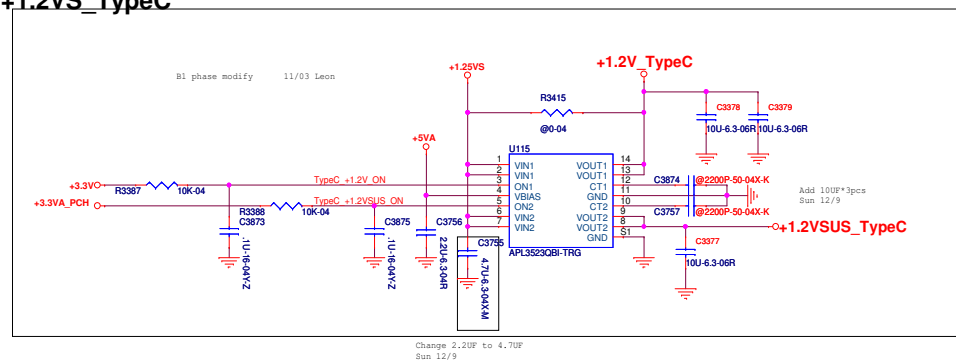
## VCCIO Converter



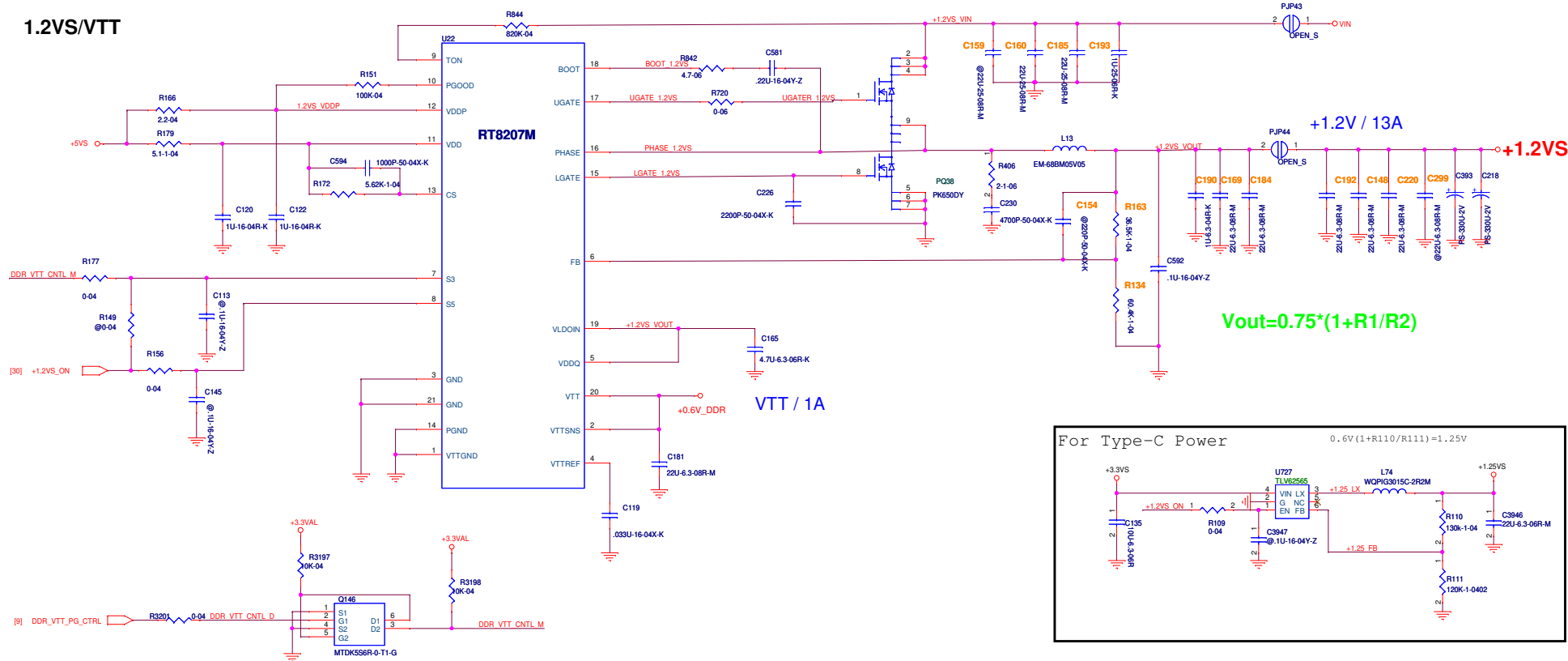
**VCCSW SUS**



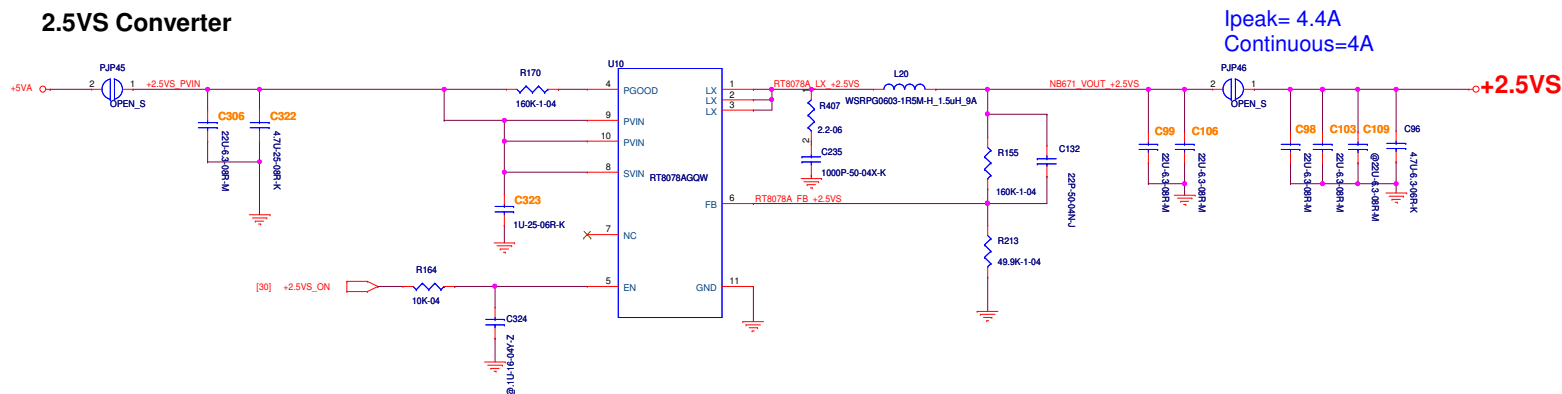
+1.2V\_TypeC  
+1.2VS\_TypeC



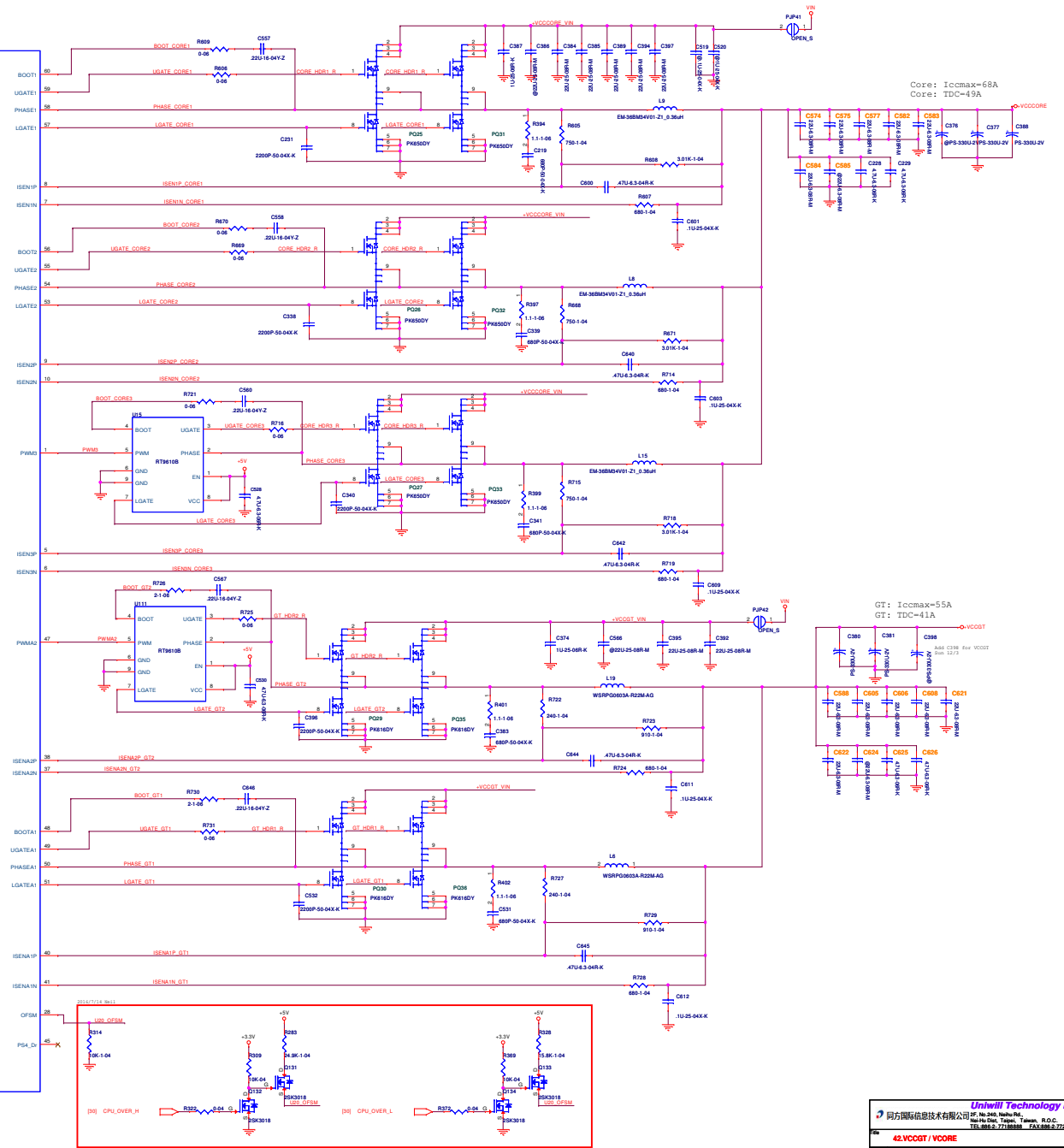
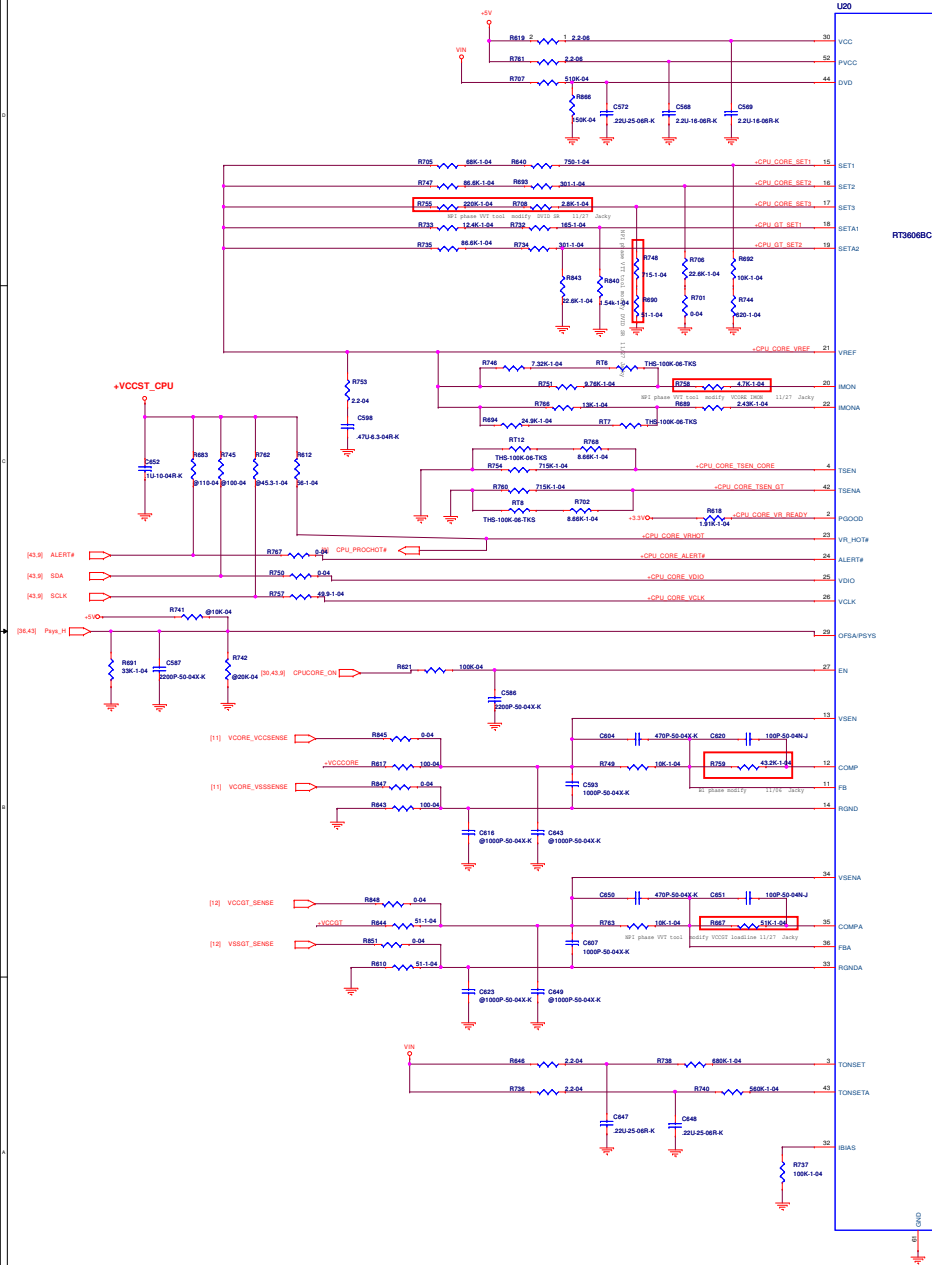
### 1.2VS/VTT



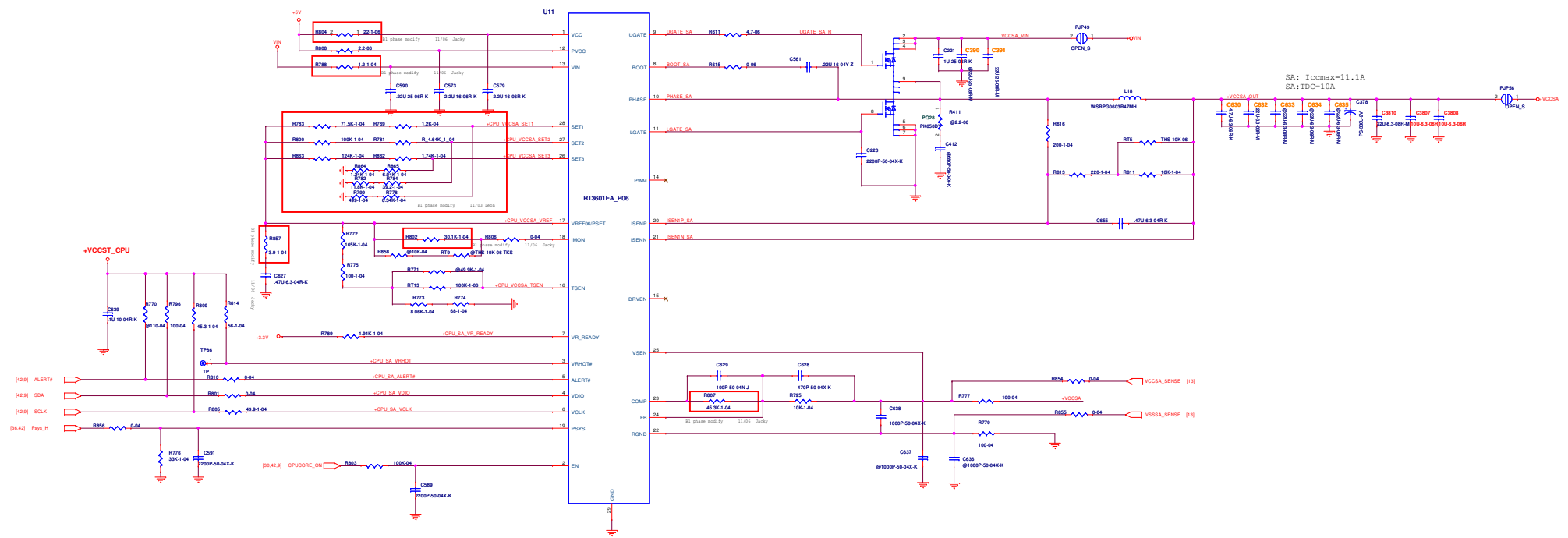
## 2.5VS Converter

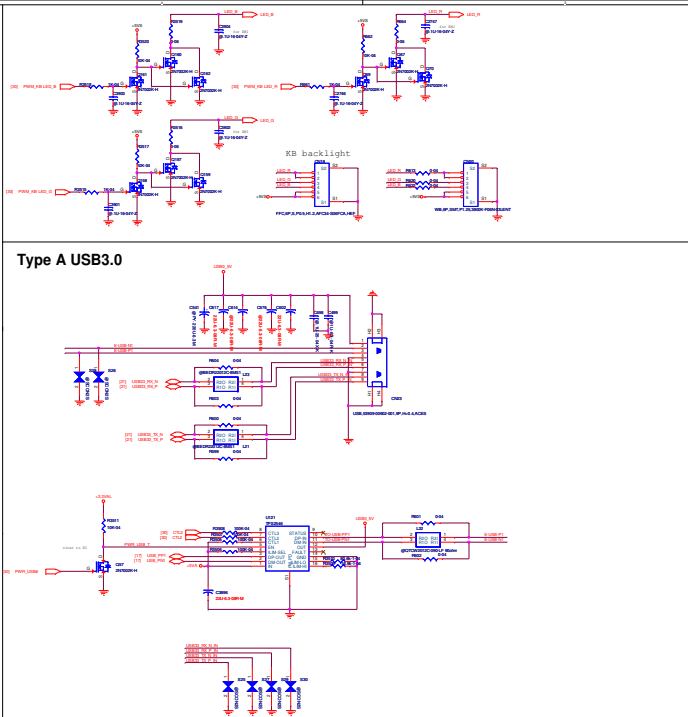
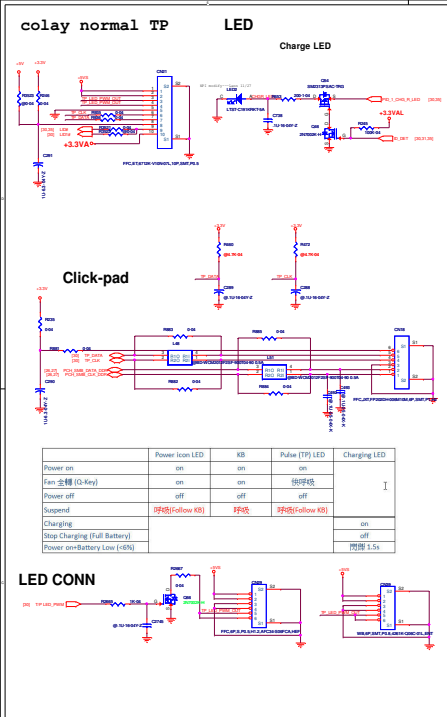


**VCCGT / VCORE**

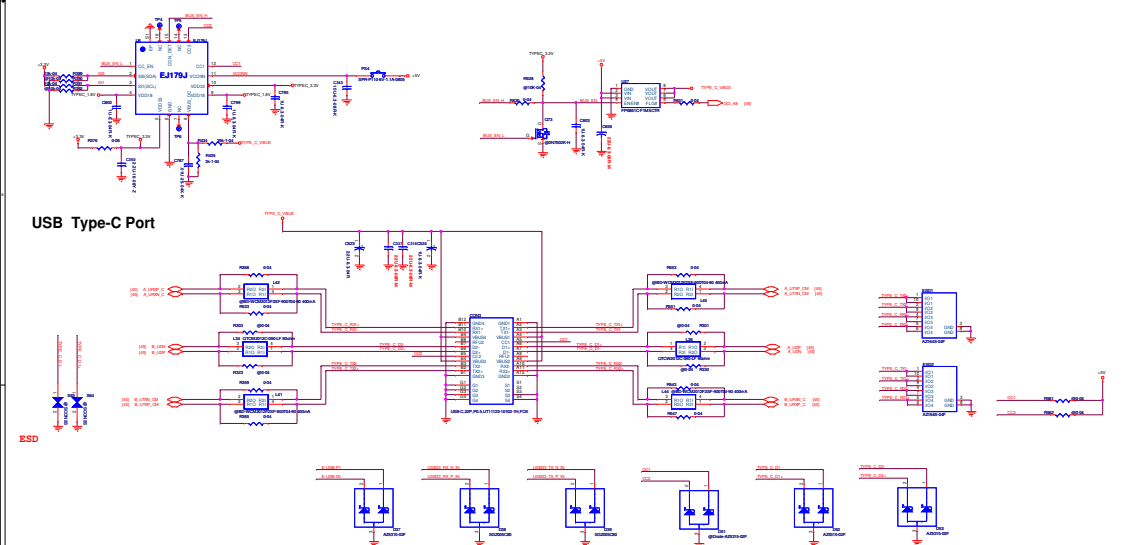


**VCCSA**

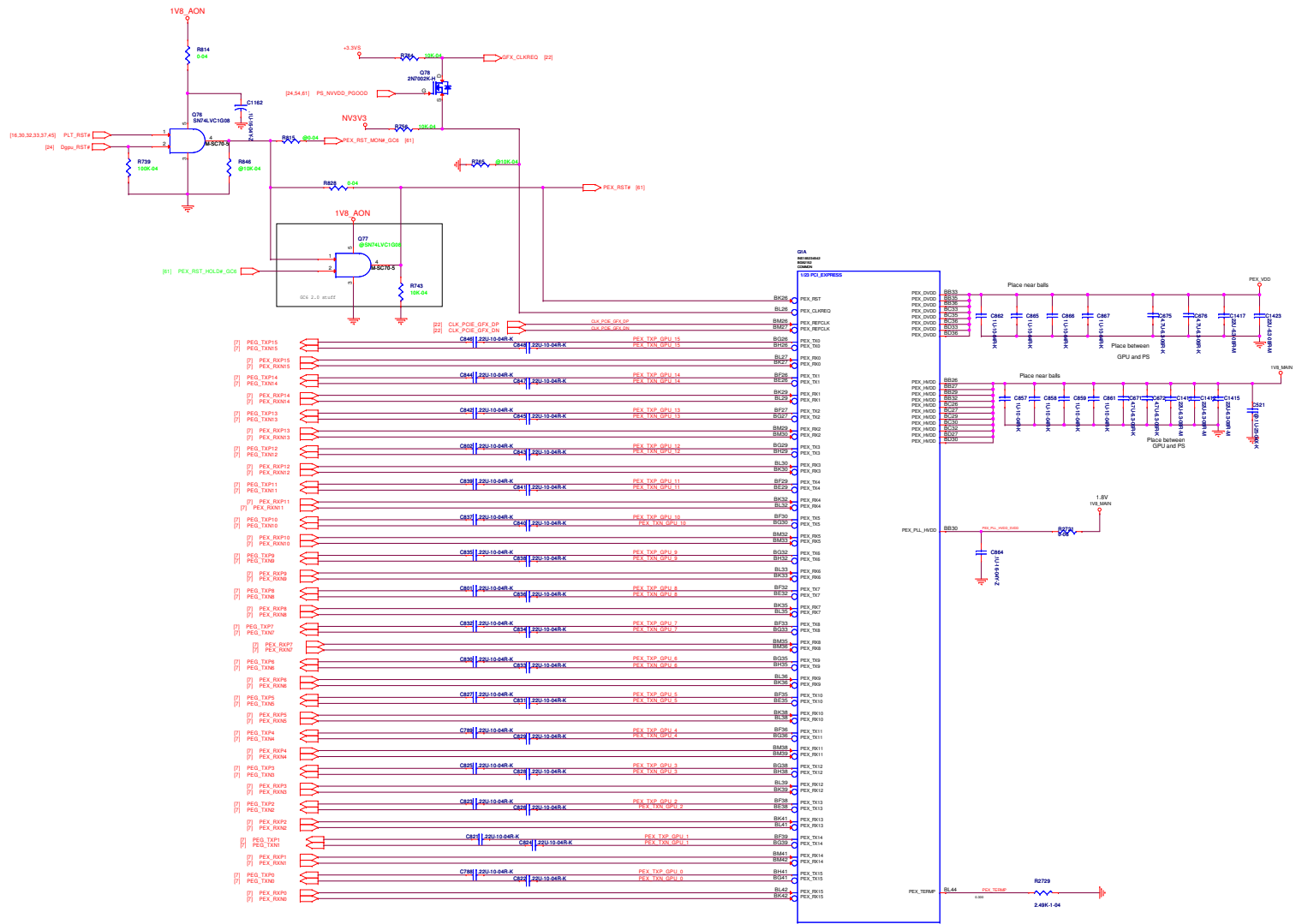


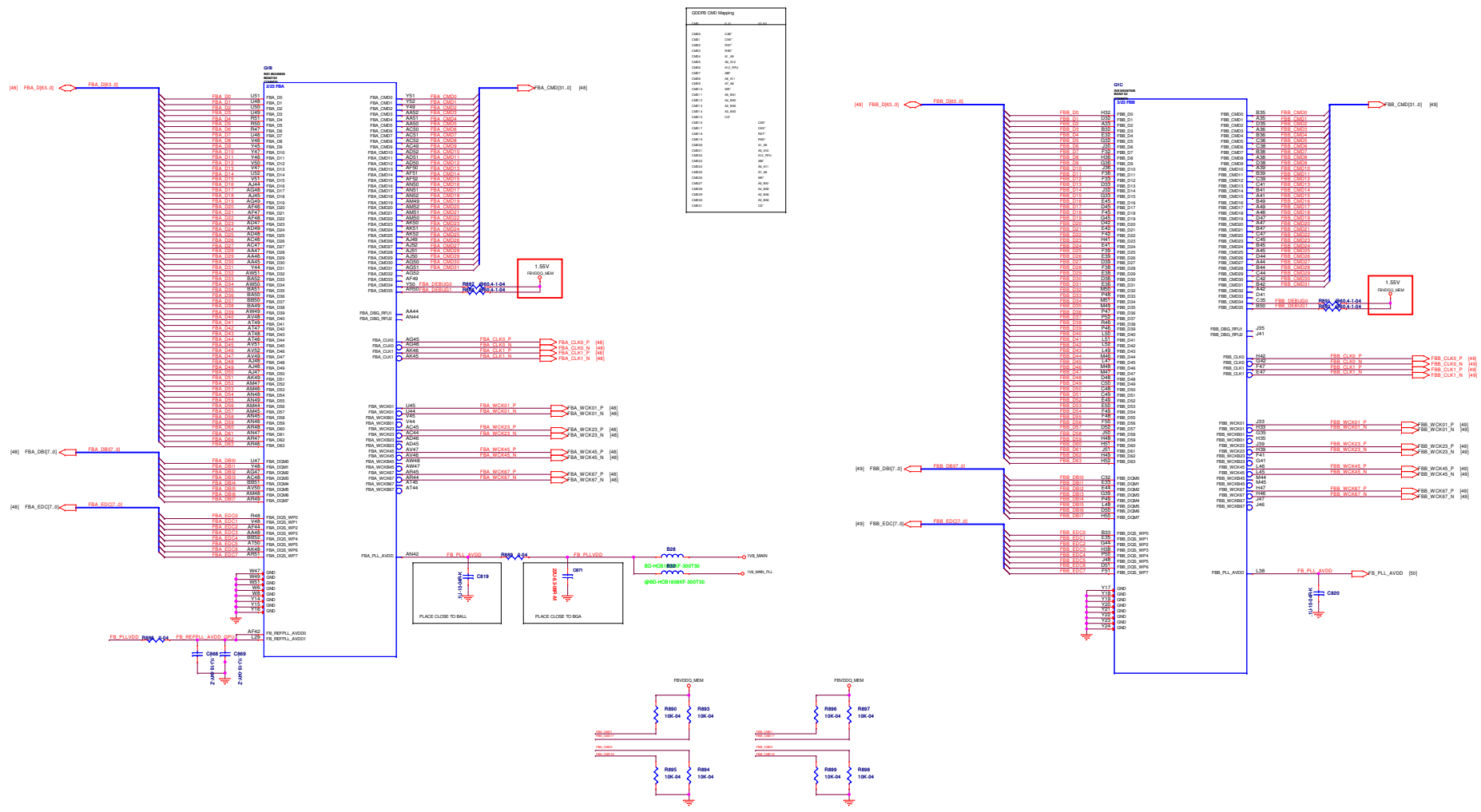


## USB Type-C SWITCH



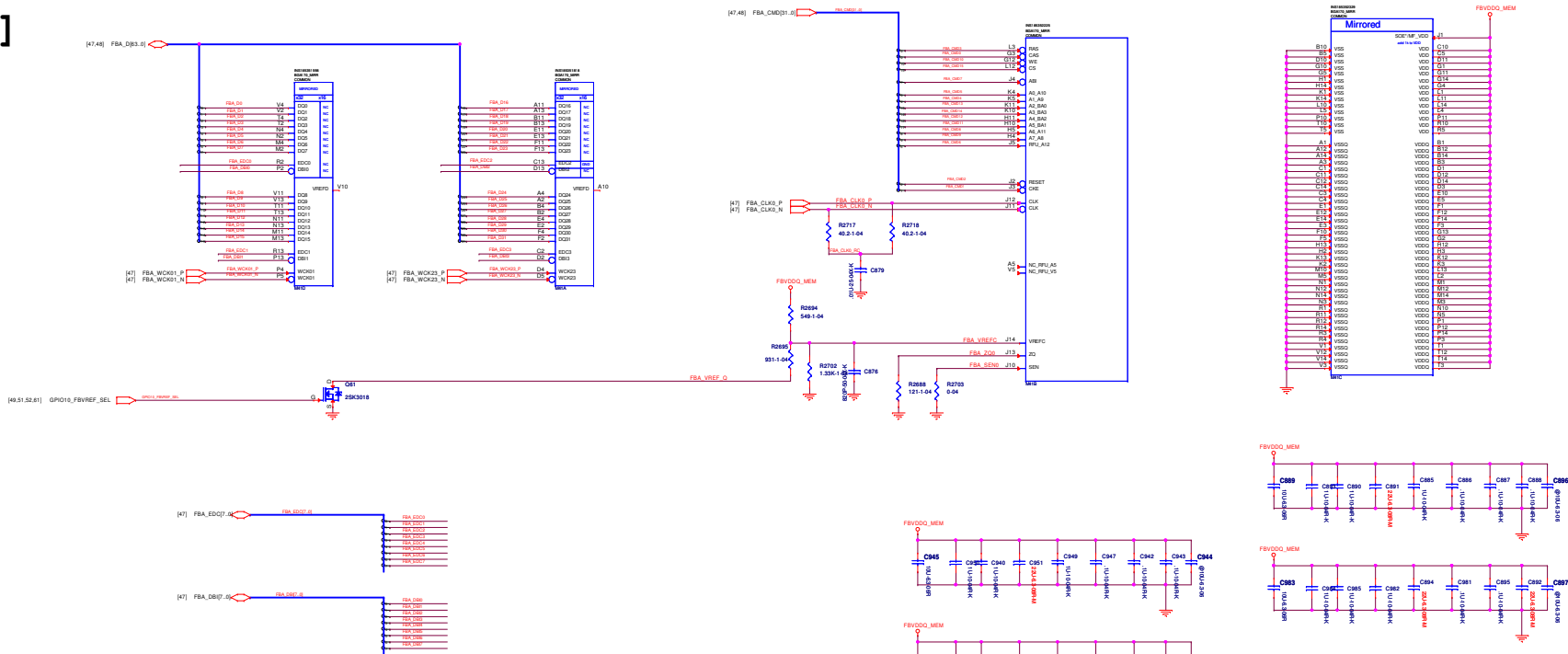




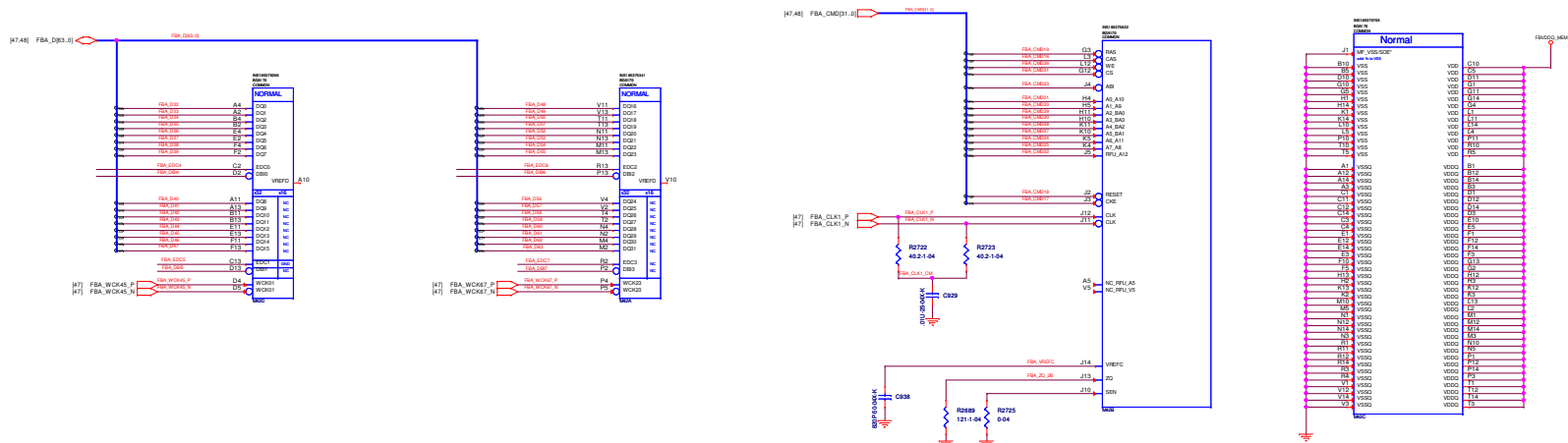


GDSII CHD Mapping	
CHD	CHD
1000	1000
1001	1001
1002	1002
1003	1003
1004	1004
1005	1005
1006	1006
1007	1007
1008	1008
1009	1009
1010	1010
1011	1011
1012	1012
1013	1013
1014	1014
1015	1015
1016	1016
1017	1017
1018	1018
1019	1019
1020	1020
1021	1021
1022	1022
1023	1023
1024	1024
1025	1025
1026	1026
1027	1027
1028	1028
1029	1029
1030	1030
1031	1031
1032	1032
1033	1033
1034	1034
1035	1035
1036	1036
1037	1037
1038	1038
1039	1039
1040	1040
1041	1041
1042	1042
1043	1043
1044	1044
1045	1045
1046	1046
1047	1047
1048	1048
1049	1049
1050	1050
1051	1051
1052	1052
1053	1053
1054	1054
1055	1055
1056	1056
1057	1057
1058	1058
1059	1059
1060	1060
1061	1061
1062	1062
1063	1063
1064	1064
1065	1065
1066	1066
1067	1067
1068	1068
1069	1069
1070	1070
1071	1071
1072	1072
1073	1073
1074	1074
1075	1075
1076	1076
1077	1077
1078	1078
1079	1079
1080	1080
1081	1081
1082	1082
1083	1083
1084	1084
1085	1085
1086	1086
1087	1087
1088	1088
1089	1089
1090	1090
1091	1091
1092	1092
1093	1093
1094	1094
1095	1095
1096	1096
1097	1097
1098	1098
1099	1099
1100	1100
1101	1101
1102	1102
1103	1103
1104	1104
1105	1105
1106	1106
1107	1107
1108	1108
1109	1109
1110	1110
1111	1111
1112	1112
1113	1113
1114	1114
1115	1115
1116	1116
1117	1117
1118	1118
1119	1119
1120	1120
1121	1121
1122	1122
1123	1123
1124	1124
1125	1125
1126	1126
1127	1127
1128	1128
1129	1129
1130	1130
1131	1131
1132	1132
1133	1133
1134	1134
1135	1135
1136	1136
1137	1137
1138	1138
1139	1139
1140	1140
1141	1141
1142	1142
1143	1143
1144	1144
1145	1145
1146	1146
1147	1147
1148	1148
1149	1149
1150	1150
1151	1151
1152	1152
1153	1153
1154	1154
1155	1155
1156	1156
1157	1157
1158	1158
1159	1159
1160	1160
1161	1161
1162	1162
1163	1163
1164	1164
1165	1165
1166	1166
1167	1167
1168	1168
1169	1169
1170	1170
1171	1171
1172	1172
1173	1173
1174	1174
1175	1175
1176	1176
1177	1177
1178	1178
1179	1179
1180	1180
1181	1181
1182	1182
1183	1183
1184	1184
1185	1185
1186	1186
1187	1187
1188	1188
1189	1189
1190	1190
1191	1191
1192	1192
1193	1193
1194	1194
1195	1195
1196	1196
1197	1197
1198	1198
1199	1199
1200	1200

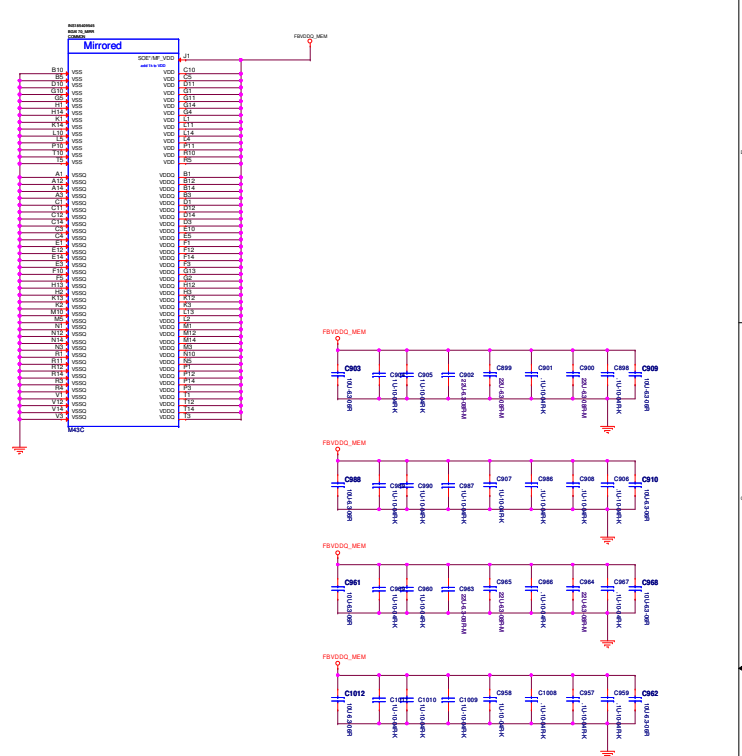
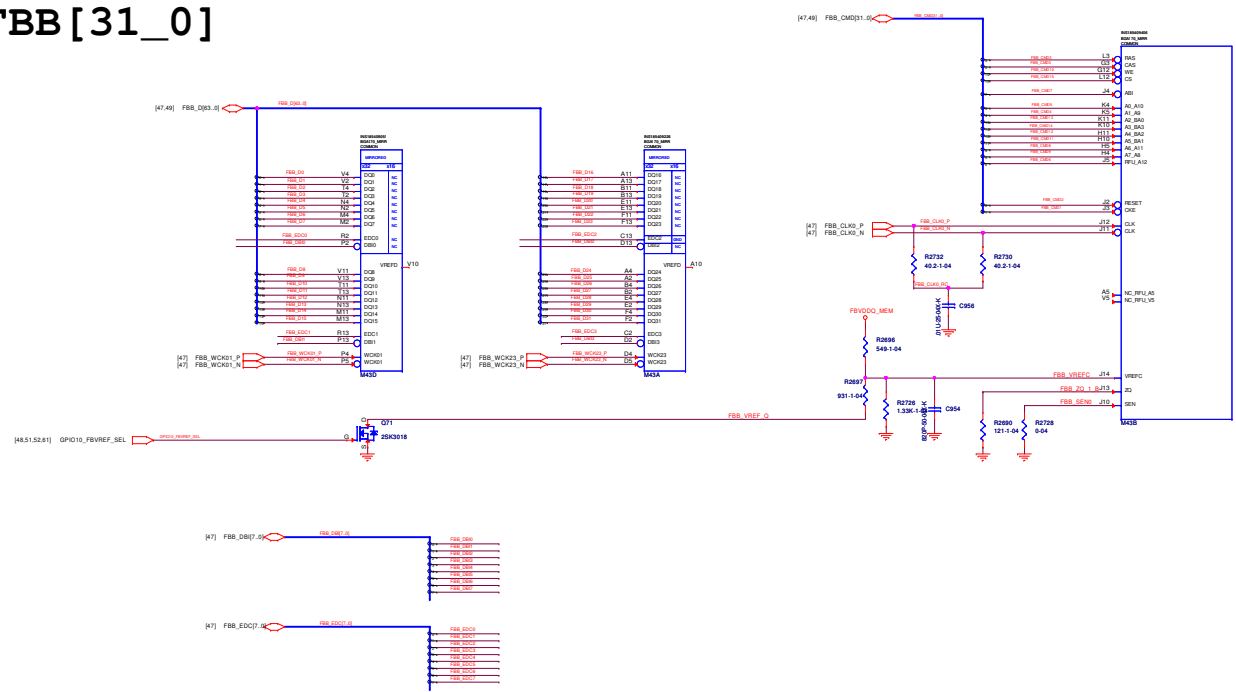
**MEM\_ FBA[31\_0]**



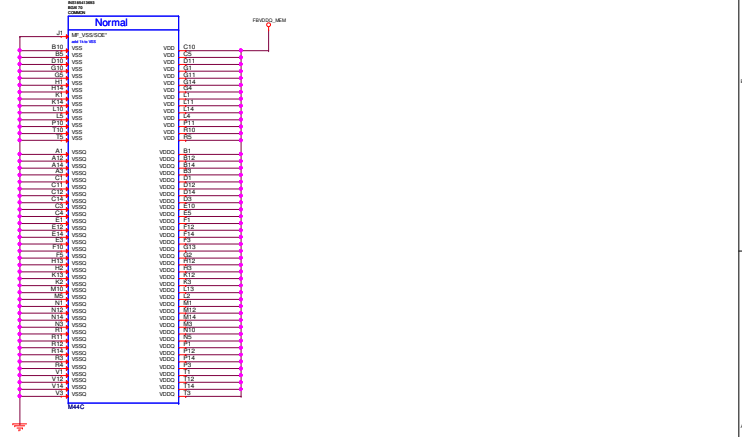
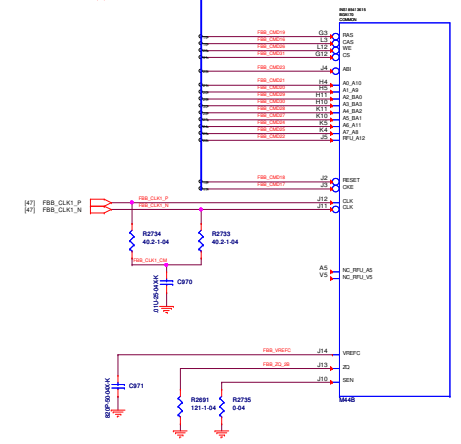
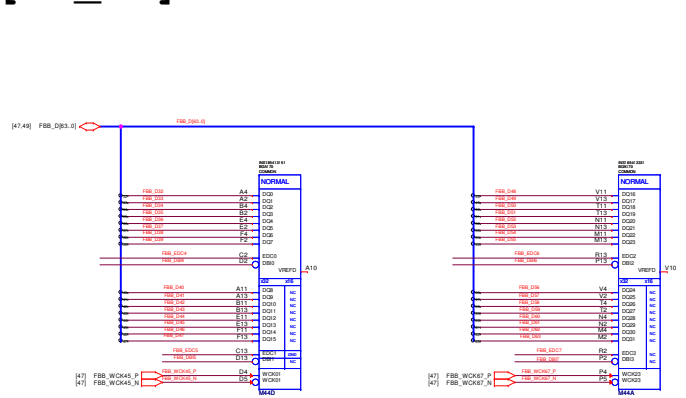
**MEM\_ FBA[63\_32]**

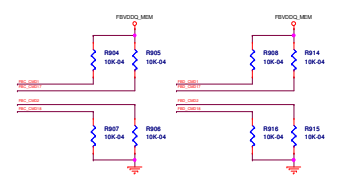
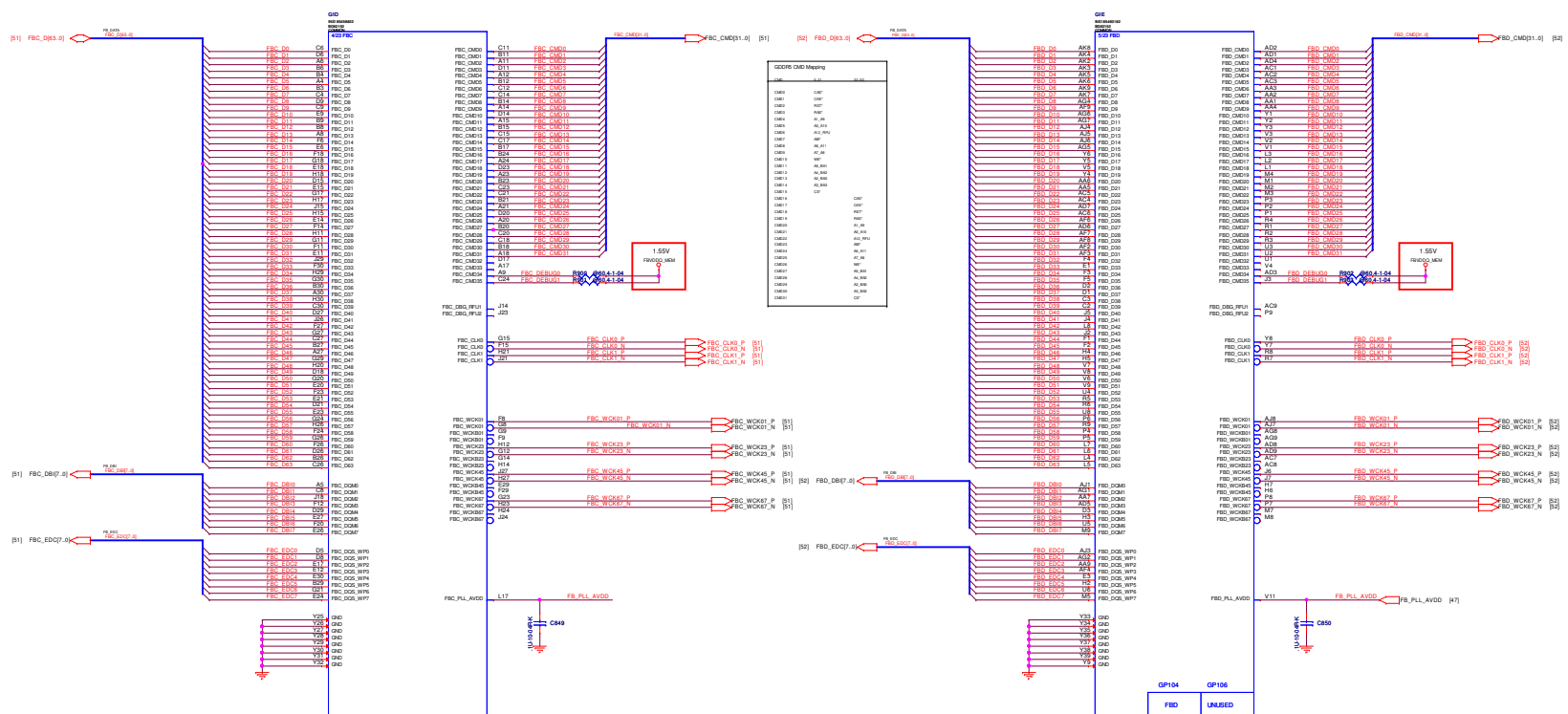


MEM\_FBB[31\_0]

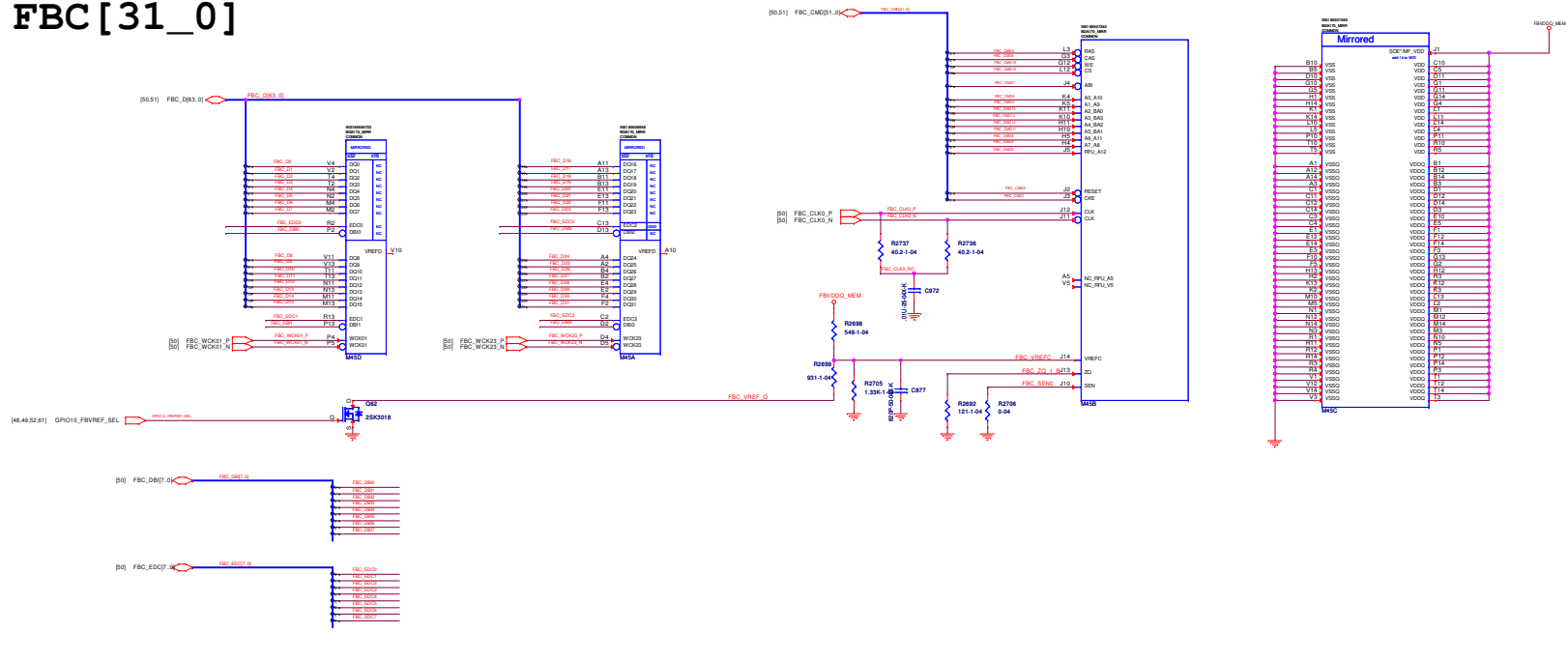


MEM\_FBB[63\_32]

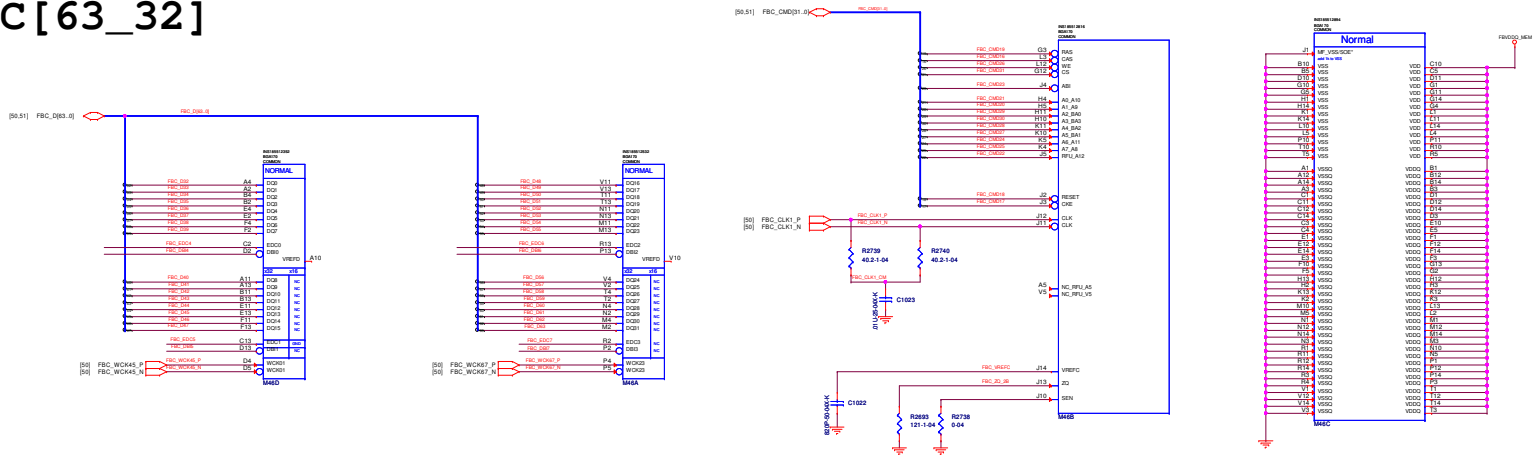




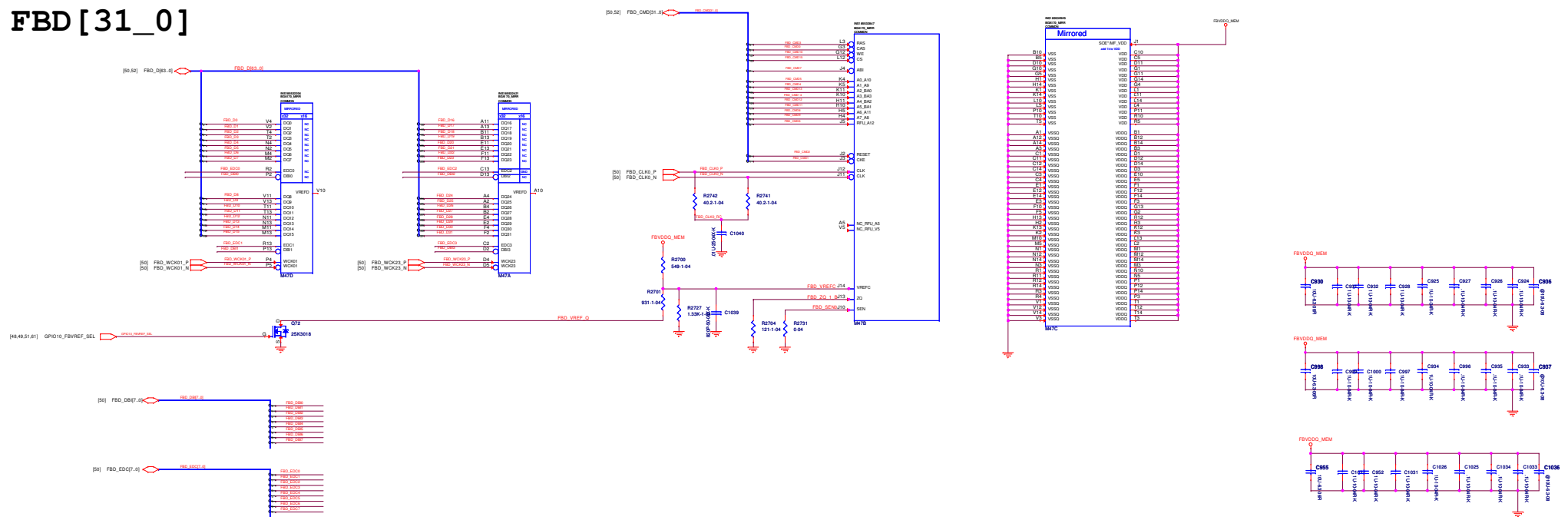
**MEM\_ FBC [31\_0]**



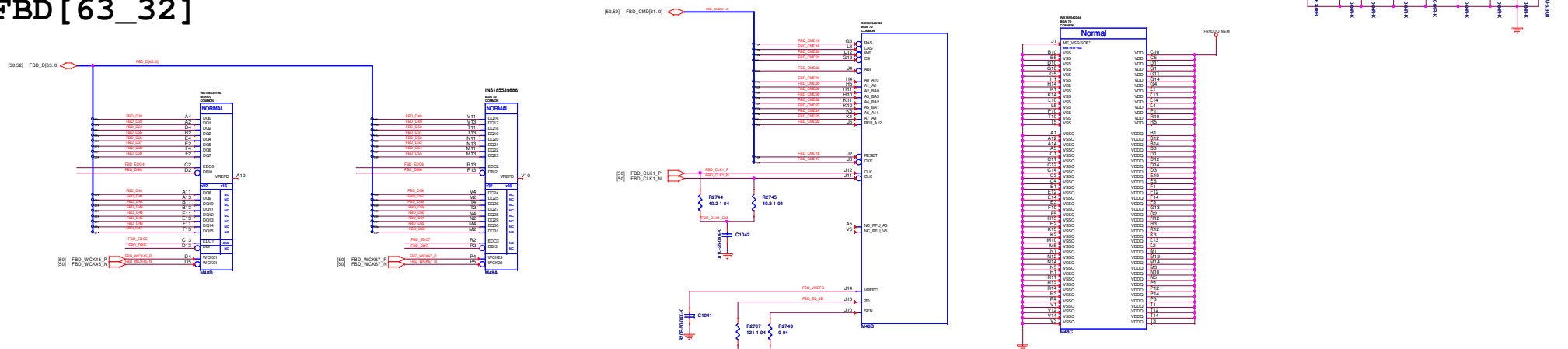
**MEM\_ FBC [ 63\_32 ]**



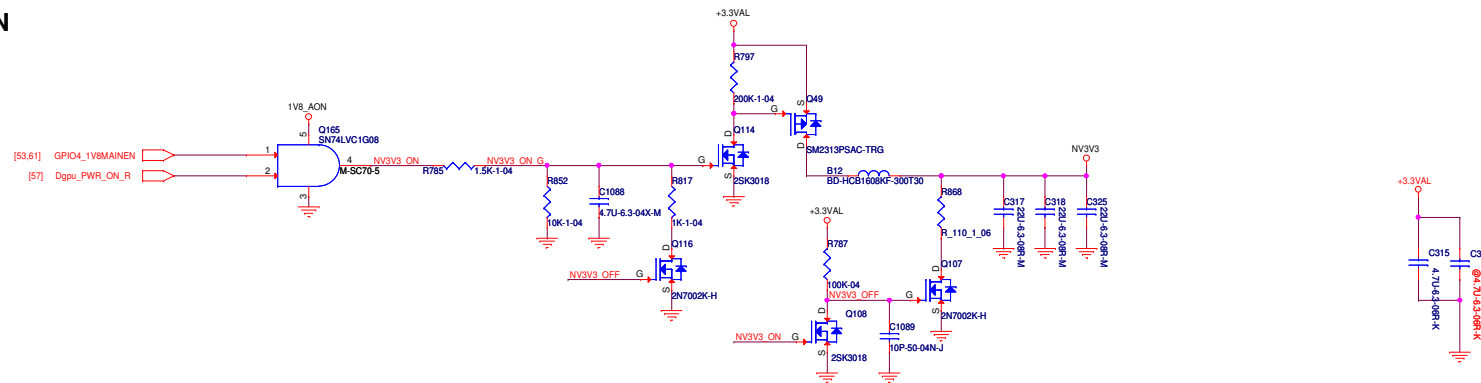
**MEM\_ FBD [31\_0]**



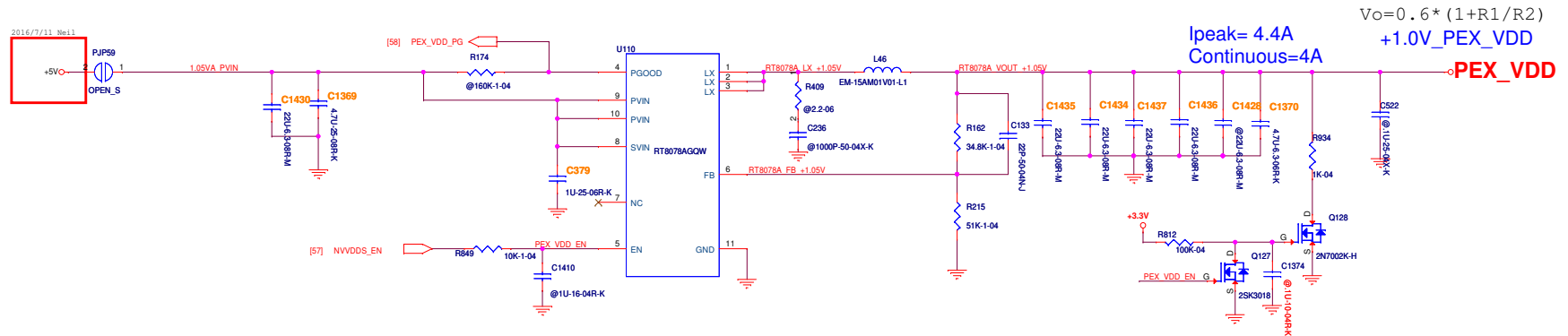
**MEM\_ FBD [63\_32]**



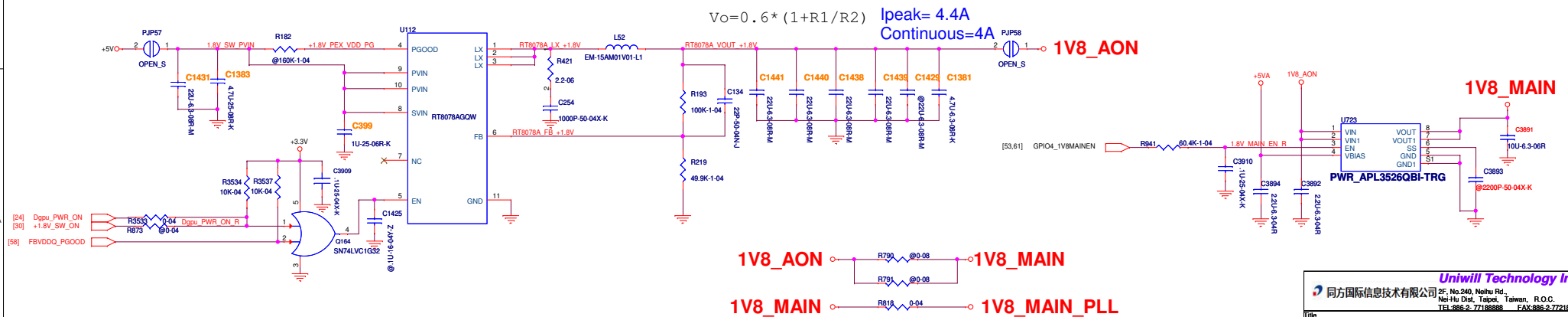
### 3V3\_AON / 3V3\_MAIN

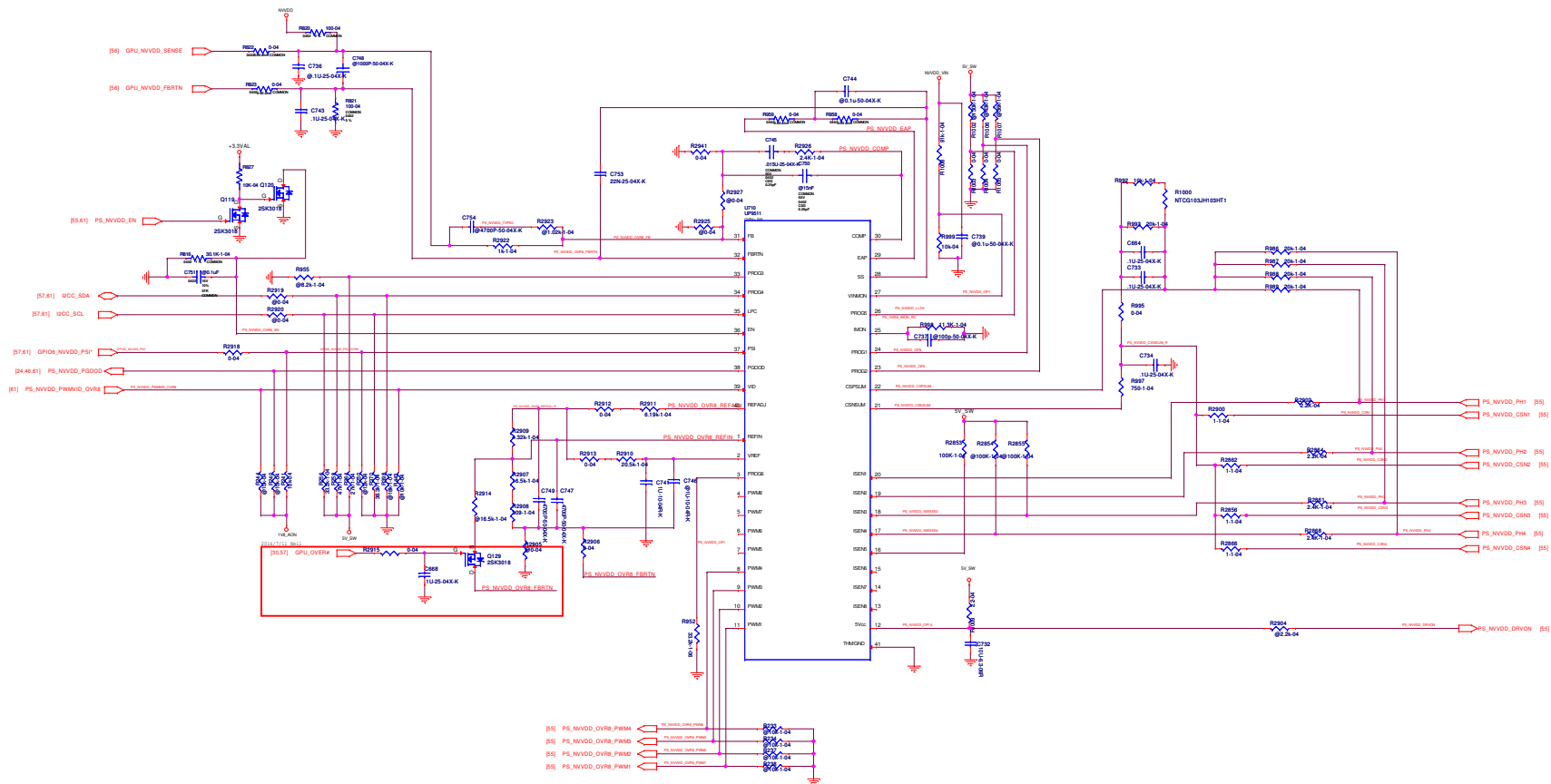


## PEX\_VDD Converter



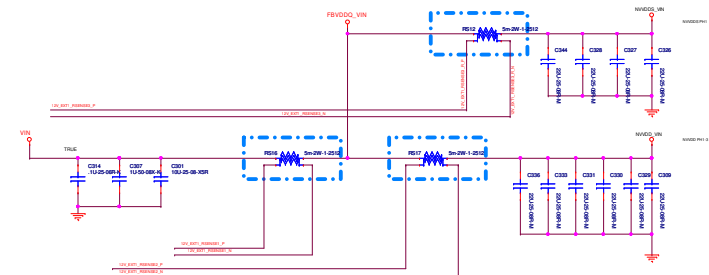
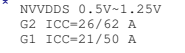
### 1.8V Converter



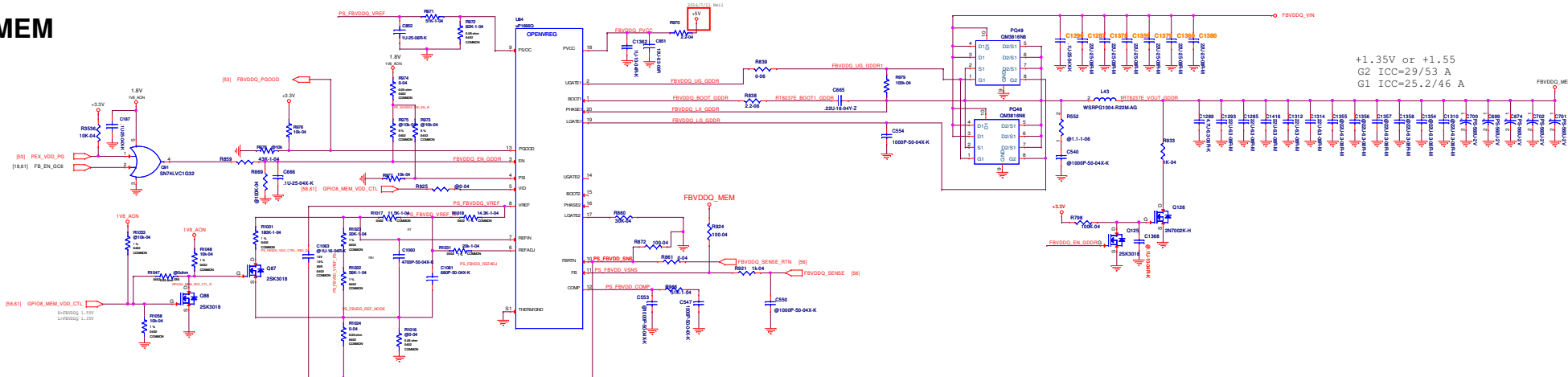








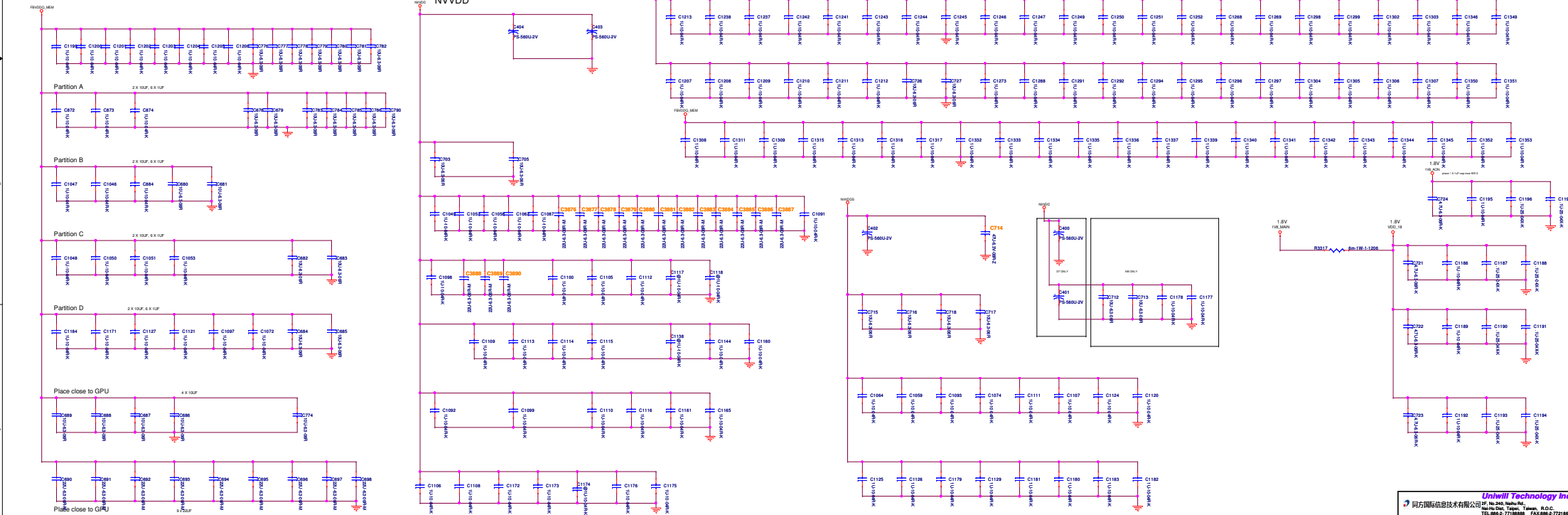
# FBVDDQ\_MEM

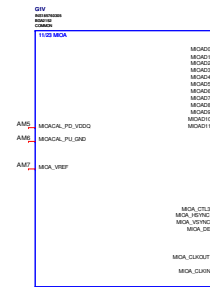
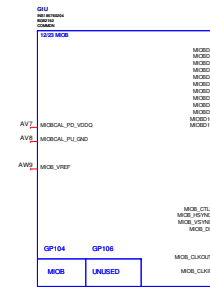
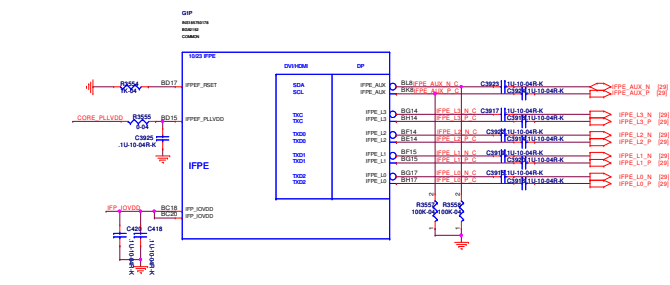
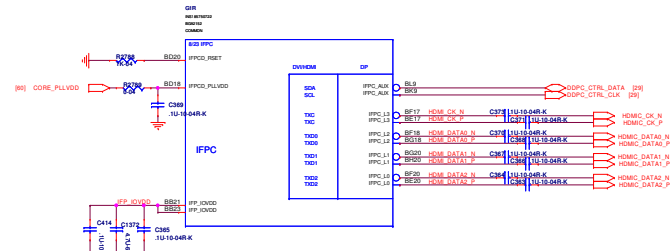
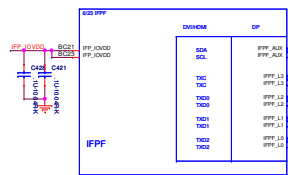
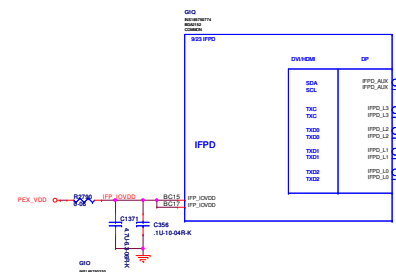
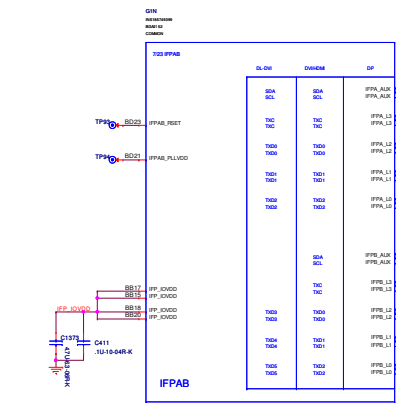


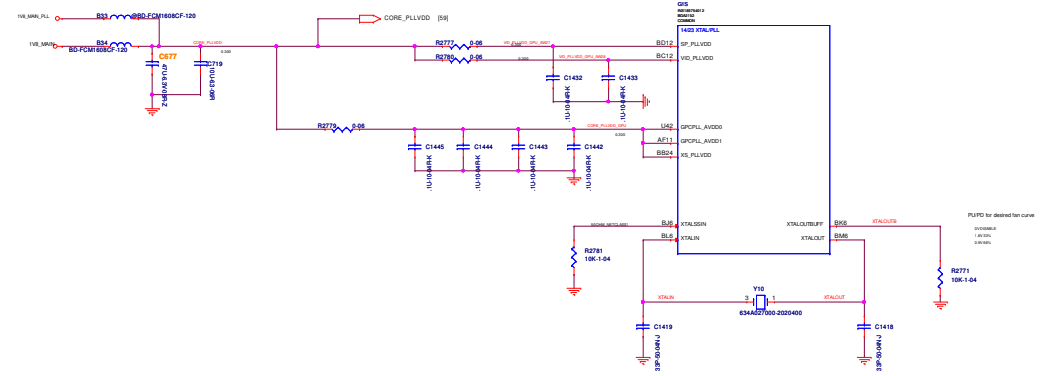
+1.35V or +1.55  
G2 ICC=29/53 A  
G1 ICC=25.2/46 A

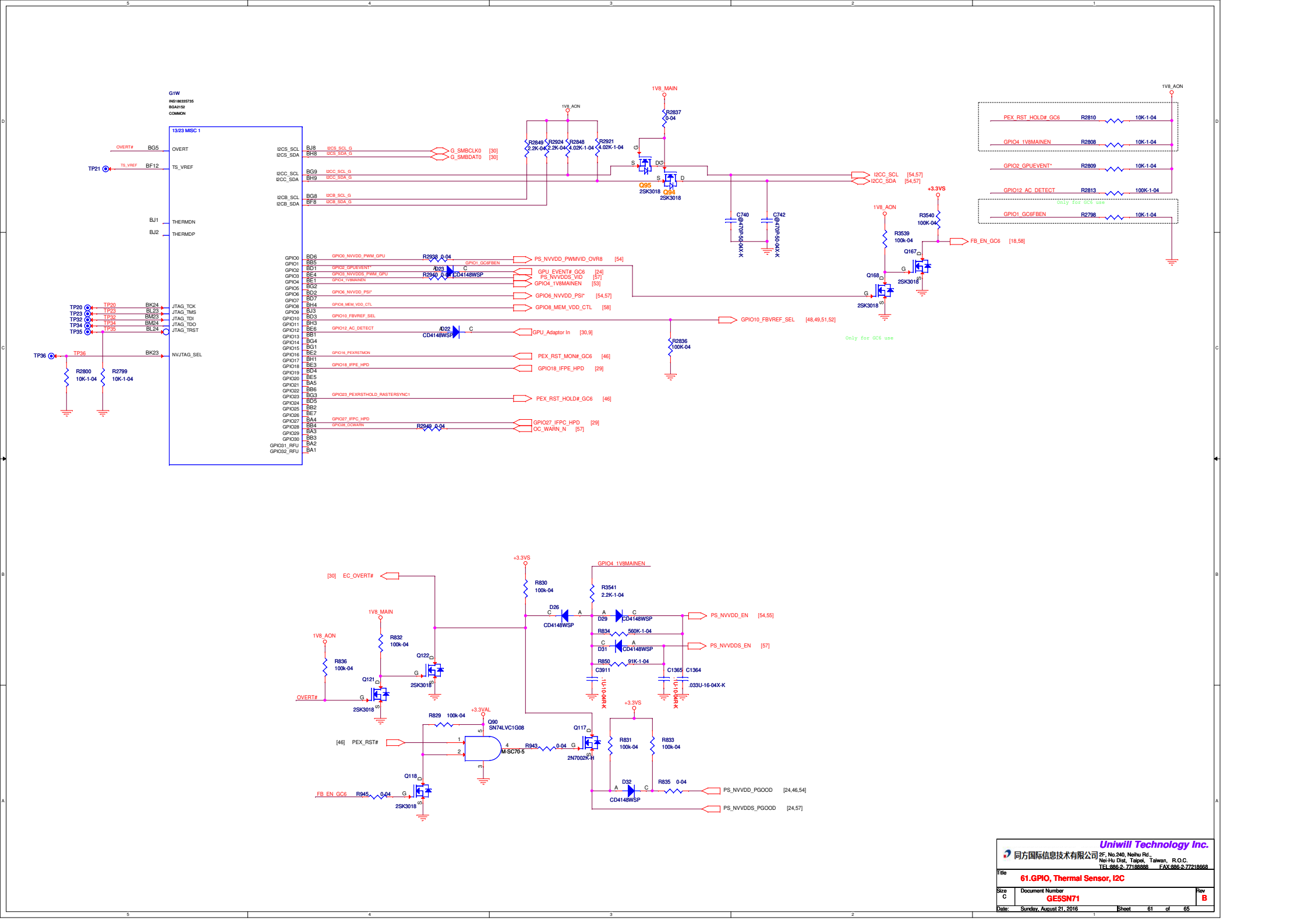
## Decoupling capacitor

FBVDDQ



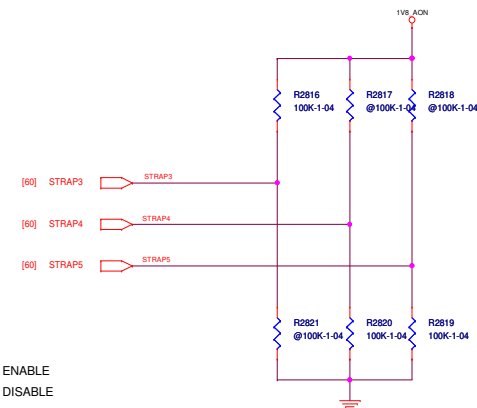
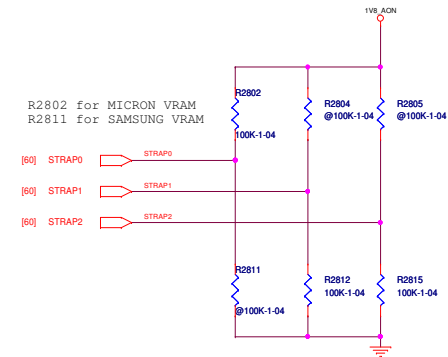






STRAP2	STRAP1	STRAP0	RAMCFG[4:0]			
L	L	L	00000			
L	L	H	00001			
L	H	L	00010			
L	H	H	00011			
H	L	L	00100			
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE		
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE		
L	L	H	1110			
L	H	L	1101			
L	H	H	1100			
H	L	L	1011			
H	L	H	1010			
H	H	L	1001			
H	H	H	1000			
L	L	M	0111			
L	M	L	0110			
L	M	H	0101			
L	H	M	0100			
H	L	M	0011			
H	M	L	0010			
H	M	H	0001			
H	H	M	0000			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

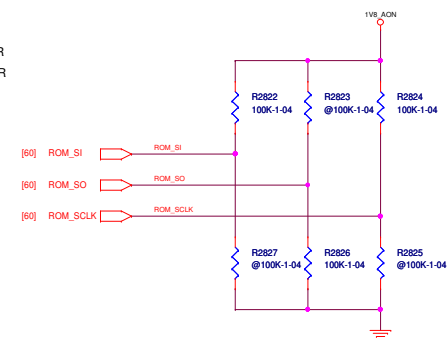


1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE

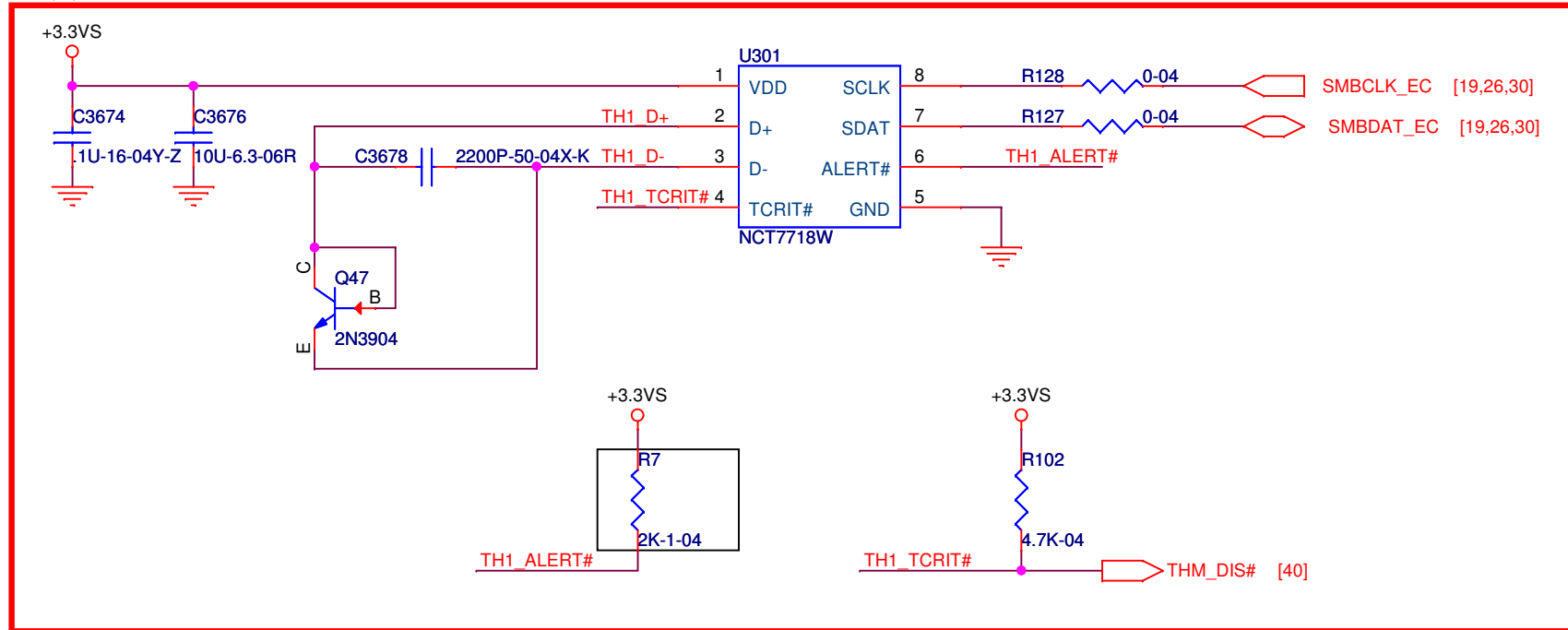
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL

1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER

1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE



2016/7/11 Neil




# ALERT# /T\_CRIT# Pull-up Resistor T\_CRIT temperature strapping point

R7	R102	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
2KΩ		77°C	87°C	97°C	107°C	117°C
7.5KΩ		79°C	89°C	99°C	109°C	119°C
10.5KΩ		81°C	91°C	101°C	111°C	121°C
14KΩ		83°C	93°C	103°C	113°C	123°C
18.7KΩ		85°C	95°C	105°C	115°C	125°C

## Layout notice:

- \*Put the C3678 2200pF to close the NCT7718W.
- \*Add ground shielding for D+ and D- traces.
- \*D+/D- route has to be away from the high noise area.
- \*The recommended traces width and ground shielding spacing are 10mils.

 <b>同方国际信息技术有限公司</b>		<b>Uniwill Technology Inc.</b> 2F, No.240, Neihu Rd., Nei-Hu Dist, Taipei, Taiwan, R.O.C. TEL:886-2- 77188888 FAX:886-2-77218668	
Title <b>63.Thermal IC/RGB</b>			
Size A	Document Number <b>GE5SN71</b>		Rev <b>B</b>
Date:	Sunday, August 21, 2016	Sheet	63 of 65

Date	Modify Content
2016/7/11	Add LOGO RGB connector(CN20)
2016/7/11	Add Thermal IC(U301) HW protection
2016/7/11	Change Q41 & Q43 from EMZB08P03H to EMB20P03H
2016/7/14	Add CPU VCORE OFSM circuit
2016/7/16	Change EC VBAT pin to +3.3VA_RTC
2016/7/18	Add EC GPA7 SUS_ON
2016/7/18	Change 5VA Buck to Richtek(RT6228C)

[illegible]

